# A 113.7 dB SINAD, 18.59 Bit ΣΔ Modulator for High-Resolution ECG Recordings

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**ABSTRACT**

**High-Resolution Electrocardiograms (HRECGs) are essential to detect low-amplitude signals in the ventricles known as "Late Potentials" that cannot be detected with a standard ECG. This work presents the design of a fully-differential second-order Cascade-of-Integrators with Feedforward (CIFF) one-bit Continuous-Time (CT) ΣΔ modulator for HRECG recordings. The modulator incorporates two active RC loop filters, a summer, and a StrongARM latch, along with a single-bit resistive DAC. Integrator and summer circuits are designed using a differential operational transconductance amplifier (DOTA). The area of the pMOS input transistors in the first-stage integrator is increased compared to that of the second-stage integrator and summer to reduce flicker noise. The StrongARM latch is implemented without using a preamplifier, leading to a reduction in area and power dissipation. The designed ΣΔ Modulator (ΣΔM) circuit achieves a high Signal-to-Noise And Distortion ratio (SINAD) and resolution through an optimal design approach and a higher oversampling ratio (OSR). The proposed ΣΔM architecture is implemented using the MATLAB delta-sigma toolbox at the system-level and the Cadence Virtuoso EDA tool at 0.18µm CMOS technology at the circuit-level. The simulated performance parameters are validated at behavioral, macromodel, and circuit levels. To measure ECG signals of 150Hz bandwidth, a 300 kHz sampling frequency ($f_s$) is used, resulting in an OSR of 1000. The proposed design achieves a SINAD of 113.7dB and a resolution of 18.59 bits. The modulator's measured power consumption is 0.49mW, achieving Schreier's Figure-of-Merit (FoM) of 168.55 dB, occupying an active area of 0.582 mm$^2$.**

***Keywords-continuous-time sigma-delta modulator; quantizer; operational transconductance amplifier; DAC***

## I. INTRODUCTION

A paradigm shift in the healthcare system is possible due to recent technological advances in low-voltage power-efficient integrated circuits, as well as innovation in sensors and wireless communications. Among several noncommunicable diseases, Cardiovascular Diseases (CVDs) are globally responsible for approximately 17.9 million deaths worldwide each year [1]. Early detection and timely treatment of CVDs prevent deaths and the need for more expensive treatment. The signals found at the end of the QRS complex or before the ST segment of an ECG waveform, as shown in Figure 1, are known as Ventricular Late Potentials (VLP). These signals have very low amplitude and high frequency, cannot be visualized with standard ECG, and require HRECG for improved diagnostic capability [2, 3]. The traditional Analog Front End (AFE) for ECG measurement comprises an instrumentation amplifier to amplify sensor output, a low-pass filter to restrict the bandwidth of noise, and a Programmable Gain Amplifier (PGA) that adjusts the amplifier gain to a level at which the Analog-to-Digital Converter (ADC) reaches its maximum SNR [3, 4]. ADCs with high resolution, ultra-low power consumption, and low input-referred noise are needed to realize robust ECG recording. In the last decade, advances in ΣΔADC design have reduced the complexity of the AFE circuit by obviating PGA and LPF blocks. ΣΔADC consists of either a Continuous-Time (CT) or Discrete-Time (DT) modulator and a decimation filter.

Many studies have attempted to improve modulator performance in terms of high precision and low power for ECG signal acquisition. In [5], a biosignal processor for a wearable

ECG device acquisition system was proposed, shifting the biosignal frequency to high frequency using a chopper to avoid flicker noise, followed by a CT feedback amplifier that drives a third-order DT High-Pass (HP) ΣΔM. This architecture used three HP integrators that increased power consumption and area. To reduce power, a third-order DTHP ΣΔM was proposed with op-amp sharing at the second and third stages with programmable feedforward coefficients [6]. The drawbacks of DTΣΔADC are that its input driver requires strict settling and slew requirements due to the switched integrators, which increase power consumption. In addition, the sampling operation limits the dynamic range value. CTΣΔM loop filters have inherent antialiasing filtering, potentially achieving higher clock frequencies and relaxing the bandwidth requirements of active elements, resulting in power savings [7, 8]. Since CTΣΔMs exhibit resistive impedance, a third-order CTΣΔM was designed in [9] to obtain high input impedance with programmable gain coefficient using a non-inverting integrator [9], which achieved a resolution of only 13 bits. In [10], a genetic algorithm was adopted for a second-order CT modulator design, achieving a resolution of 15 bits. In [11], a flexible AFE was proposed with an active-RC loop filter using a fully differential difference amplifier for the first stage, followed by a passive integrator and second-order CTΣΔM design in [12] using an active RC integrator to achieve a resolution of 17 bits. This study presents a high-DR–high-resolution CTΣΔM for ECG signal acquisition.

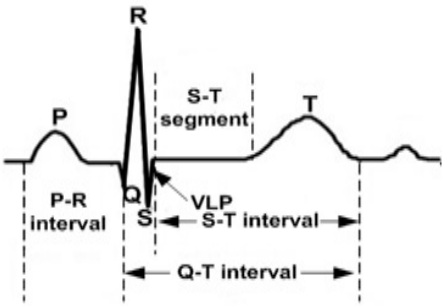


Fig. 1. ECG waveform.

## II. CT ΣΔM ARCHITECTURE

Figure 2 depicts the block diagram of the second-order CIFF structure. It consists of a CT-type loop filter, summer, one-bit quantizer, and DAC. The advantages of the CIFF architecture are that it uses a single feedback DAC, provides a stable closed-loop system, processes only the quantization noise, and provides lower signal swings at each loop filter output [13].

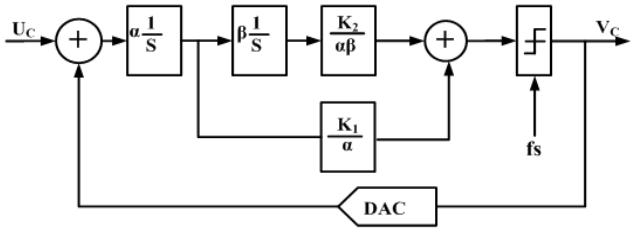


Fig. 2. Second-order CTΣΔM with FF structure.

The behavioral modeling is implemented in MATLAB, with simulations performed using Schreier's Delta-Sigma toolbox [14]. With a two-level quantizer, OBG of 1.5, and OSR of 1000:

$$NTF\ (z)\ = \frac{Z^2-2Z+1}{Z^2-1.219Z+0.4477} \quad (1)$$

Figure 3 shows the measured output spectrum, depicting an in-band SNR of 117.26 dB with ENOB of 19.19, and exhibiting a slope of 40 dB/decade that confirms the second-order noise-shaping.

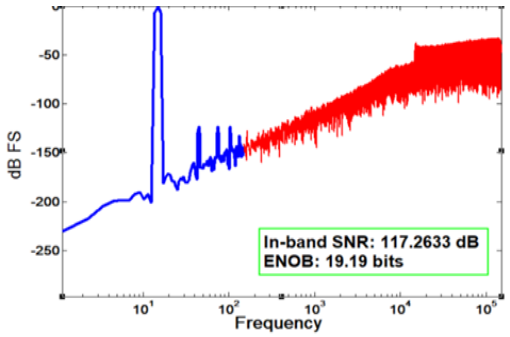


Fig. 3. Measured output spectrum.

## III. CIRCUIT DESIGN OF SECOND-ORDER CTΣΔM

Figure 4 illustrates the schematic of the proposed FF second-order CTΣΔM with a 2-level quantizer and a resistive DAC.

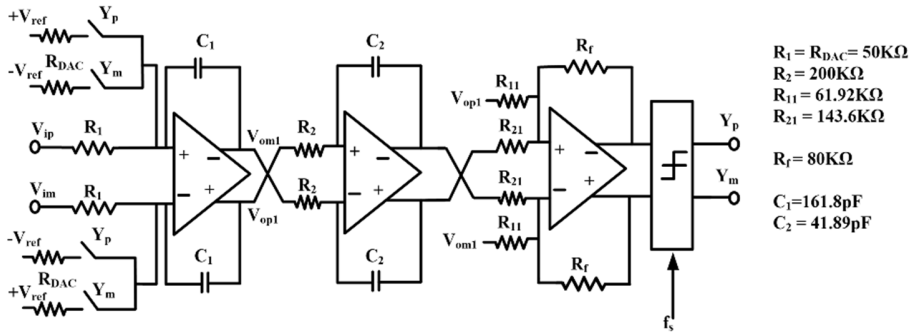


Fig. 4. Schematic of the proposed second-order CTΣΔM.

The FF design in the loop only processes in-band quantization noise, which reduces the output swing across each integrator, relaxing the operational amplifier requirements. It also avoids peaking in the signal transfer function [15, 16]. Usually, the amplifier circuit with the clock signal uses the chopper modulation method to effectively reduce $1/f$ noise at a cost of additional clock circuitry and switches, increasing power consumption along with circuit complexity [17]. In this work, to minimize $1/f$ noise, DOTA uses the pMOS input stage, and the first-stage integrator's input transistors' area is increased compared to that used in the second-stage integrator and summer. The loop filters are realized by an active RC integrator. The RC time constant of integrators is determined using:

$$f_s = \frac{1}{\alpha R_1 C_1} \text{ and } f_s = \frac{1}{\beta R_2 C_2} \quad (2)$$

The in-band and DAC signals are processed by the first-stage integrator. To attain better matching performance and lower thermal noise, $R_1$ is chosen to be equal to $R_{DAC}$. The first stage uses a resistor of 50 kΩ and a capacitor of 161.8 pF. The second-stage integrator is set with a larger resistor and a smaller capacitor. A resistor of 200 kΩ in the second stage reduces the area of the capacitor using 41.89 pF. In the summer circuit design, the K-coefficients, $K_1 = 0.6667$ and $K_2 = 0.2288$ are employed, as determined using the Delta-Sigma toolbox. The summing amplifier adds up both FF branches, followed by a dynamic latch-based comparator to perform quantization. The single-bit resistive DAC in the feedback loop uses the signals $Y_p$ and $Y_m$. One of the non-idealities in a high-speed CTΣΔM that can lead to instability in the modulator is excess loop delay, which arises from the nonzero switching time of the DAC transistors and the quantizer. However, in low-speed applications, this is not a major concern, as the duration of a single clock period is sufficiently long, and the time delay is only a small fraction of one clock cycle [18]. Figure 4 shows the design of all resistors and capacitors. The input-referred-voltage-noise spectral power density for the circuit in Figure 4 is:

$$v_{n,in}^2 = v_{n,R_1}^2 + v_{n,R_{DAC}}^2 + v_{n,op}^2 + v_{n,s}^2 \quad (3)$$

where $v_{n,R_1}^2$, $v_{n,R_{DAC}}^2$, $v_{n,op}^2$, and $v_{n,s}^2$ is the contribution of input resistance, DAC resistance, opamp, and the second-stage integrator, respectively. The expression for each is as follows,

$$v_{n,R_1}^2 + v_{n,R_{DAC}}^2 = 16kTR_1 * SBW \quad (4)$$

$$v_{n,op}^2 = \frac{8kT\gamma}{g_{m,1}}\left[1 + \frac{g_{m,3}}{g_{m,1}}\right] * SBW * \left[1 + \frac{R_{DAC}}{R_1}\right]^2 \quad (5)$$

$$v_{n,s}^2 = 8kTR_2\,(2\pi fRC_1)^2 * SBW \quad (6)$$

The integrated-input-referred-noise-power in SBW is,

$$P_n = \frac{2kT\gamma}{C_c}\left[1 + \frac{g_{m,3}}{g_{m,1}}\right] * \frac{1}{OSR} \quad (7)$$

where $k$, $T$, $C_C$, $g_m$, and $SBW$ are the Boltzmann constant, absolute temperature, compensation capacitor, amplifier input transconductance, and signal bandwidth, respectively. The reset switch $kT/C$ noise resets the integration capacitor for a short time, and it is negligible for typical values of $C$~100 pF and $g_m$~1 mS [19]. Furthermore, the gain of the first-stage integrator suppresses the noise from the second-stage one.

### *A. Differential OTA*

The main blocks of the SDM circuit that require operational amplifiers are the integrators and the summer, which are the main sources of power consumption. In this work, Miller-compensated two-stage DOTA is used, since it provides better linearity, larger DC gain, reduced in-band noise, and wider output swing compared to other topologies, such as inverter-based, bulk-driven, folded-cascode, rail-to-rail, and telescopic [20-22]. In the proposed DOTA, the main amplifier is a two-stage current mirror, a Common-Mode-Feedback (CMFB) circuit is CT to maintain the output level stability, and the output stage is class-AB to attain increased current efficiency and larger output driving capability and transient speed [21]. Figure 5 shows the circuit schematic of the DOTA used in the circuit of Figure 4. The two-stage DOTA uses a 1.8 V supply and a 1 μA current source to bias the circuit. The fully differential input stage consists of transistors $M_1$ to $M_4$, in which pairs $M_1$-$M_2$ and $M_3$–$M_4$ have identical device sizes. Since flicker noise dominates at low frequencies, to reduce it, pMOS transistors are used at the input stage, and also the first-stage DOTA input transistors' area is increased compared to the DOTA used in the second-stage and summer circuits.

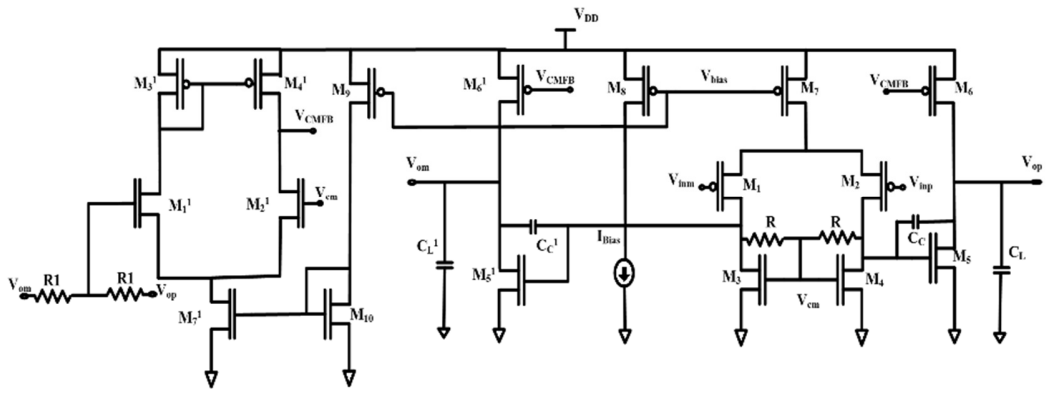


Fig. 5. Schematic of DOTA.

The non-inverting input ($V_{inp}$) and inverting input ($V_{inm}$) are applied at $M_1$ and $M_2$, respectively. Transistor $M_8$ is the current source of the differential stage, with a bias current ($I_{bias}$) of 1 µA. The differential currents, along with the first-stage output resistance, generate a single-ended output voltage that drives the second-stage. The nMOS common source amplifier $M_5$-$M_5^1$ and pMOS current source load $M_6$-$M_6^1$ form a second stage that provides additional gain. A Miller capacitor, $C_c$ of 4 pF, is connected between both stages to ensure loop stability and to obtain a phase margin more than 45° [21, 22]. The design parameters of all the MOSFETs and $C_C$ were adjusted during the Cadence design process to achieve the desired performance. The tolerable minimum input signal that drives the input pair out of saturation is,

$$V_{in,min} = 0.2\,V \geq -|V_{GS1,2}| + |V_{dsat1,2}| + V_{GS3,4} \quad (8)$$

where $V_{GS}$ is the gate-source voltage and $V_{dsat}$ is the minimum drain-source voltage required to maintain transistor saturation. The input common-mode voltage swing is approximately 0.2 to 1.6 V. The input-referred thermal noise density is,

$$v_{n,op}^2 = \frac{8kT\gamma}{g_{m,1}}\left[1+\frac{g_{m,3}}{g_{m,1}}\right] * SBW * \left[1+\frac{R_{DAC}}{R_1}\right]^2 \quad (9)$$

The first-stage CMFB is employed by a large resistor R connected between the drains of $M_3$ and $M_4$, with a midpoint biasing their gates. Fully DOTA's common-mode output voltage is stabilized using a CMFB circuit consisting of $M_1^1$, $M_2^1$, $M_3^1$, $M_4^1$, and $M_7^1$ transistors. The loop gain of the CM loop is almost the same as the two-stage DOTA, and Miller $C_C$ ensures the stability of the loop. The resistors R = 2 MΩ and $R_1$ = 200 kΩ are used to leave the DC gain unaffected. The CM error amplifier, via its output $V_{CMFB}$, adjusts the DOTA CM output voltage by controlling the gates of $M_6$ and $M_6^1$. The current consumption of the CMFB amplifier is 10 µA. The voltage gain ($A_v$) and the Gain-Bandwidth-Product (GBW) of the designed DOTA are:

$$GBW = \frac{g_{m1}}{C_c} \text{ and}$$

$$A_v = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right) * \left(\frac{g_{m5}}{g_{ds5}+g_{ds6}+G_L}\right) \quad (10)$$

where $g_{mi}$ is the transconductance of a specific transistor and $G_L$ is the load transconductance. The transistors that share the same gate were scaled based on the current in the transistor, and the lengths were maintained the same to minimize the offset. Input transistors were biased to keep all the transistors in saturation. Table I shows the dimensions of each transistor in the circuit.

Figure 6 exhibits the frequency response with the gain and phase of the designed DOTA at the first and second stages. To ensure the stability of ADCs in biomedical applications, the DOTA needs to have a phase margin greater than 45° and a gain of 60 dB. Table II reports the simulated performance of the designed DOTA. It is clear that increasing the size of the input transistors reduces noise; however, this occurs with the trade-off of higher power consumption and a larger chip area.

TABLE I. SUMMARY OF THE DOTA TRANSISTOR SIZING.

| Device name | $W$ (µm) | $L$ (µm) | $I_D$ (µA) | $g_m$ (µS) |
|---|---|---|---|---|
| $M_1$ and $M_2$ | 5 | 0.3 | 4.95 | 77.7 |
| $M_3$ and $M_4$ | 4 | 4.8 | 4.95 | 47.7 |
| $M_5$ and $M_5^1$ | 24 | 4.8 | 30.4 | 302.64 |
| $M_6$ and $M_6^1$ | 29.7 | 1.19 | 30.4 | 279 |
| $M_7$ | 9.99 | 1.19 | 9.9 | 86.77 |
| $M_8$ | 0.99 | 1.19 | 1 | 8.48 |
| $M_1^1$and $M_2^1$ | 25 | 4.8 | 4.91 | 85.59 |
| $M_3^1$and $M_4^1$ | 4.95 | 1.19 | 4.91 | 43.26 |
| $M_7^1$and $M_{10}$ | 10 | 1 | 9.83 | 165.29 |
| $M_9$ | 9.9 | 1.19 | 9.9 | 86.04 |

TABLE II. PERFORMANCE COMPARISON OF THE DESIGNED DOTA

| Parameter | 1st stage | 2nd stage |
|---|---|---|
| DC gain in dB | 81.85 | 74.35 |
| UGB in MHZ | 8.31 | 6.78 |
| Phase margin | $53.2^0$ | $54.37^0$ |
| Power consumption in µW | 184.15 | 101.2 |
| Input referred noise in µV/$\sqrt{Hz}$ | 1.89 | 18.63 |

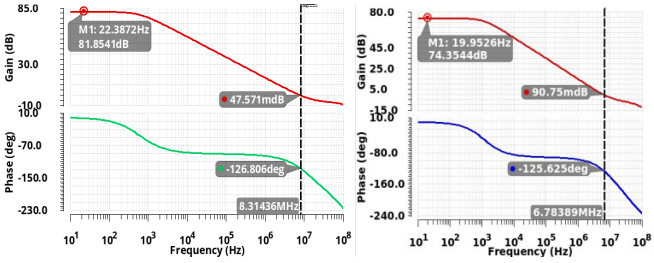


Fig. 6. Frequency response of the first and second stage DOTA.

## B. *Quantizer*

The designed latch is implemented without a preamplifier, resulting in reduced area and, consequently, lower power consumption. Figure 7 illustrates the circuit diagram of a StrongARM latch as a comparator, which consists of a clocked differential pair ($M_1$, $M_2$), two precharge switches ($S_1$, $S_2$), a cross-coupled pMOS pair ($M_5$, $M_6$), and a Set-Reset (SR) latch formed by two NAND gates. The Strong-ARM latch has the following characteristics: it consumes zero static power, has an input-referred offset derived from input pairs $M_1$ and $M_2$, and generates rail-to-rail outputs [23, 24]. When the CLK is at a low level, the latch enters reset mode, and transistors $M_1$, $M_2$ are turned off with all the nodes above the differential pair pulled to $V_{DD}$, and the SR latch preserves the previous state of the regeneration phase. With CLK at high level, the latch will be in regenerative mode with switches $S_1$, $S_2$ turned off and $M_1$, $M_2$, and $M_3$ turned on, drawing differential current proportional to the difference of $V_{inp}$ and $V_{inm}$. The imbalance in pull-down current from the differential pair is amplified through positive feedback provided by $M_5$ and $M_6$, until either S or R goes low, which in turn sets (resets) the latch to produce the required output digital signal. The SR latch reduces the occurrence of metastability by keeping its outputs (0 or 1) during a long regeneration time [25]. Also, the drive of the pMOS pair is kept stronger than the nMOS input pair to prevent metastability. Switches $S_1$ and $S_2$ suppress dynamic offsets by removing the previous states at drains of $M_1$-$M_2$. An initial $V_{DD}$ voltage is

established at the drains of $M_1$-$M_2$, which allows amplification before the differential pair enters the triode region. As the clock frequency is low in this design, the delay of the designed latch is not important. To reduce on-resistance and charge injection, all transistors are used at the shortest length [26].

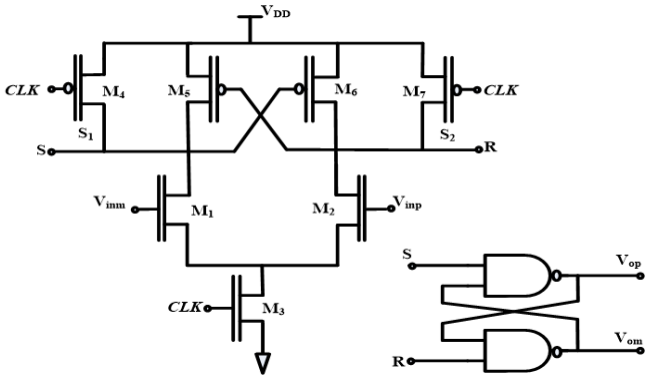


Fig. 7. Schematic of a single-bit quantizer.

### C. Feedback DAC

The DAC in the feedback comprises a resistive unit element of 50 kΩ, as shown in Figure 8. The reference voltages $V_{refp}$ and $V_{refm}$ drive the resistors in the feedback. The other terminals of the resistors are connected to a transmission gate that acts as a switch and are connected to the virtual ground of the first integrator. $Y_p$ and $Y_m$ are the outputs of the quantizer.

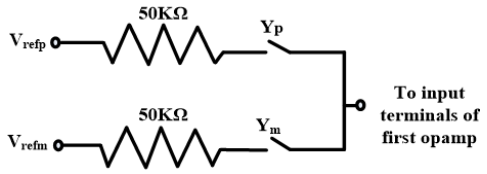


Fig. 8. DAC unit element.

### D. Switches

The switches used in Figures 4 and 8 are transmission gates. They are carefully designed to ensure the lowest ON resistance, with $L_n = L_p = 0.18\ \mu m$, $W_n = 2\ \mu m$, and $W_p = 4\ \mu m$.

### E. Layout Details

The proposed 180nm CMOS second-order CT ΣΔM was implemented using Metal-Insulator-Metal (MIM) capacitors, polyresistors, and standard $V_t$ transistors. The common centroid layout technique was used in all blocks. Figure 9 shows the layout, where the integrators, summer, and quantizer are highlighted. The first-stage integrator takes the majority of the space, due to the use of large input transistors to reduce flicker noise. The modulator occupies a silicon area of 0.582 $mm^2$ (864×674 µm).

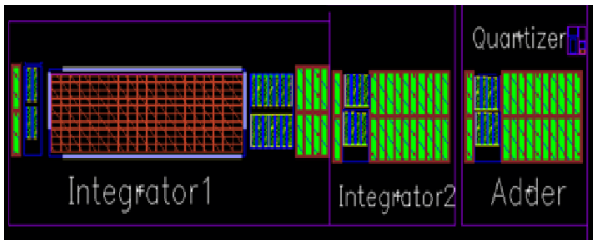


Fig. 9. Layout of the CTΣΔM.

## IV. EXPERIMENTAL RESULTS

Due to the periodic nature of ECG signals, the inherent noise can be reduced by enhancing the signal component, which in turn improves overall signal resolution and aids in the detection of late potentials. The proposed second-order CTΣΔM was implemented using 0.18 µm CMOS technology with a supply voltage of 1.8 V. An input sinusoidal signal of 0.25 V at 91.55 Hz is applied to the modulator, having an $f_s$ of 300 kHz and an OSR of 1000. The output for a sine wave input is a pulse-density modulated wave. For a Hanning window of 16384 points, the modulator achieves a SINAD of 113.7 dB and a DR of 112 dB for a BW of 150 Hz. The ENOB is 18.59 with a power consumption of 0.49 mW, achieving a Schreier FOM of 168.55 dB. Figure 10 shows the resulting power spectral density of the designed modulator. Figure 11 shows the modulator SNDR versus normalized input signal amplitude, providing a peak SNR of 92.43 dB and a DR of 112 dB.

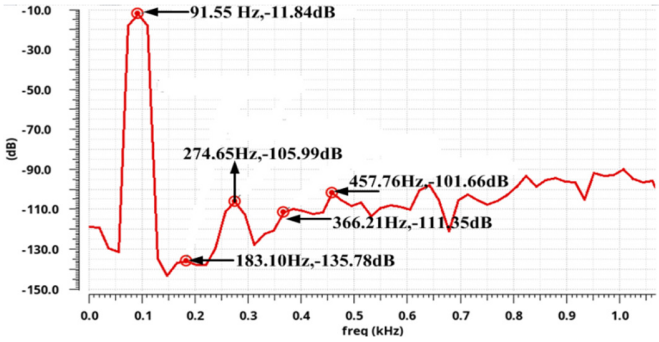


Fig. 10. Power spectral density of the designed modulator.

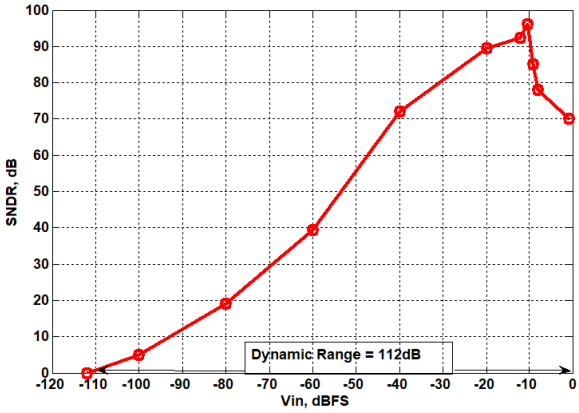


Fig. 11. Measured SNDR vs input voltage.

Table III summarizes the measured results of the proposed work and other state-of-the-art methods for an 180 nm technology node. It can be observed that the proposed work exhibits higher resolution and SINAD compared to other ΣΔMs designed for low-bandwidth applications.

TABLE III. PERFORMANCE SUMMARY AND COMPARISON

| | **[27]** | **[10]** | **[6]** | **[18]** | **[28]** | **Proposed** |
|---|---|---|---|---|---|---|
| Architecture | DT | CT | DT | CT | CT-DT | CT |
| $V_{pp}$ | 1.8 | 1 | 1.8 | 1.8 | 1.8 | 1.8 |
| Bandwidth | 20 kHz | 2 kHz | 200 Hz | 250 Hz | 500 Hz | 150 Hz |
| $f_s$ (KHz) | 1024 | 1024 | 25.6 | - | 500 | 300 |
| SINAD (dB) | 70 | 100 | 80 | 81.4 | 101 | 113.7 |
| Power (μW) | 20 | 32.34 | 5.2 | 2.16 | 63 | 490 |
| ENOB (bits) | 10.75 | 15.37 | 13 | 12.73 | 16.48 | 18.59 |
| FoMs (dB) | 156.48 | 177.9 | 140.7 | 162.03 | 160.1 | 168.55 |

## V. CONCLUSION

This study presented a single-bit second-order CTΣΔM for HRECG recordings, using an active-RC integrator with a two-stage pMOS input DOTA and resistive-feedback DAC to suppress noise. Flicker noise is further reduced by enlarging the first-stage integrator's input transistor area relative to the subsequent stages. Power and area are minimized by eliminating the preamplifier in the single-bit StrongARM latch and opting for a lower-order loop. The excess loop delay is ignored because of its negligible impact relative to the clock period. At an $f_s$ of 300 KHz and an OSR of 1000, for an input signal of 0.25 V and 91.55Hz, the modulator achieves a highest SINAD of 113.7dB and a resolution of 18.59 bits. The proposed modulator is appropriate for use in the detection of cardiac late potentials in HRECGs, which has significant clinical implications.

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