Low Power High Speed Finfet Dram Cell and 4x4 Array Design Using the Sleep Transistor Technique

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ABSTRACT

Dynamic Random-Access Memory (DRAM) is a key element in high-performance digital systems, but conventional designs suffer from high power dissipation and latency. This paper presents three new FinFET-based DRAM cell architectures: a two-transistor (2T) DRAM and two three-transistor (3T) DRAM configurations, each of which incorporates sleep transistors to enhance energy efficiency. The proposed designs aim to optimize read and write delay while reducing both dynamic and short-circuit power consumption. FinFET devices improve switching speed, and the inclusion of sleep transistors effectively minimizes leakage, enabling lower overall energy use. Circuit-level simulations were carried out in the Cadence Virtuoso Analog Design Environment. The results demonstrate that the proposed 2T-DRAM achieves a 66% reduction in write delay, while the 3T-DRAM achieves up to 98% improvement in read delay. Power consumption decreases by up to 99.6% during writing and 99.8% during reading operations compared to conventional DRAM cells. These outcomes highlight the effectiveness of the proposed FinFET-based DRAM architectures for compact, low-power on-chip memory applications.

Keywords-DRAM; 2T-DRAM; 3T-DRAM; power; delay

I. INTRODUCTION

Memory is an integral component of any digital system or device. It is important to design memory cells that are efficient in terms of delay, Power Performance, and Area (PPA) [1]. High performance is one major factor, while power is a significant problem faced worldwide today [2]. DRAM is primarily chosen because of the simplicity of its cells and their eligibility, as opposed to its Static Random-Access Memory (SRAM) alternatives. For a smaller number of transistors (<4), DRAM can store more data than SRAM in the same chip size [3]. Basic DRAM cells are developed using low-power design approaches, such as sleep mode to reduce leakage power [4]. In order to preserve data, DRAM must be refreshed regularly [5], and the binary information is stored in DRAM memory cells as stored charges on capacitors. Leak currents gradually deplete the battery, necessitating a refresh procedure [6]. The rapid increase in leakage power dissipation stems from scaling technology to the nanometer scale (static and dynamic power dissipation) [7]. Reducing static power waste during periods of inactivity has become essential for developing design approaches [8]. A power decrease is required without sacrificing performance, which makes it more difficult to limit leakage during normal operation. Several approaches are employed in sleep or standby states to decrease leakage power [9]. Power gating is a well-known method in which a sleep transistor is placed between virtual ground and the real ground rail. The rapid development of nanoscale devices has made reducing energy consumption a major challenge for Very-Large-Scale Integration (VLSI) designers and researchers [10, 11]. Due to the rapid expansion of the electronics industry, the modeling of TFTs and the capacity to simulate circuit behavior prior to production are crucial [12]. Planar MOSFETs, which are sensitive to RDF, have been replaced by FinFETs below the 22-nm technology node, because FinFETs have greater gate controllability. This controllability suppresses Short Channel Effects (SCE) without requiring significant channel doping, allowing tolerance of process variation [13]. FinFETs have a greater write and read yield than planar MOSFETs due to their larger on-current and reduced variability. Furthermore, FinFET displays preferable outcomes compared to CMOS in terms of latency, power-delay product, and energy delay product [14]. FinFET improves propagation latency by 10.03 times, and is quicker than CMOS, so the power-delay and energy-delay products are lower than those of CMOS.

A. Coventional 2T-DRAM

Figure 1 shows a conventional 2T DRAM circuit using FinFETs. During write operations, Write Wordline (WWL) is low and based on the Write Bitline (WBL) value, the storage capacitor is charged or discharged. During the read operation, WWL is low and Read Bitline (RBL) is high when a '0' or a '1' is read; it is then switched on [15].

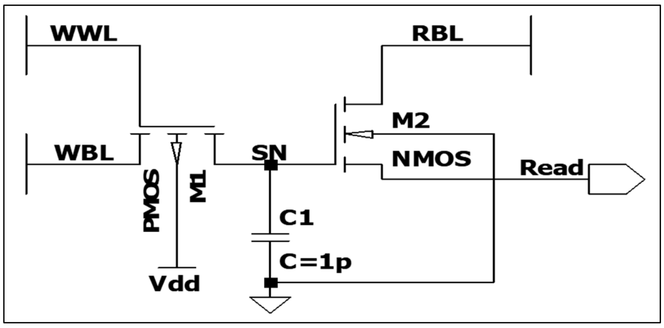

Fig. 1. Conventional 2T-DRAM design.

B. Coventional 3T-DRAM

Figure 2 depicts a conventional 3T-DRAM circuit that uses FinFETs, consisting of three nFETs, a capacitor, and voltage sources for the read and write operations. For the write operation, when WWL is high and RWL is low, the value on BL is fed to the storage capacitor. For the read operation, the value of the storage capacitor is detected at the BL2 line [16].

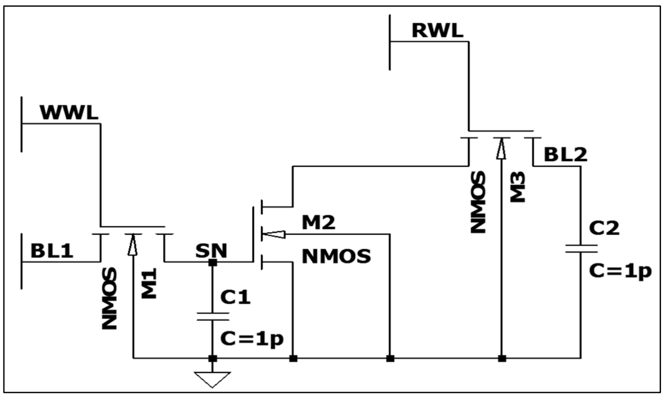

Fig. 2. Conventional 3T-DRAM design.

The design of the basic DRAM cells (2T-DRAM and 3T-DRAM) uses FinFETs and low-power design strategies, such as sleep mode, to reduce leakage power. These transistors split the circuit's power network into two: a permanent network linked to the power source and a virtual network that supplies energy to the cells and can be switched off. As a result, leakage power decreases significantly.

II. PROPOSED DESIGNS

A. Methodology

In PPA, the aim is to reduce power and optimize speed/delay. The methodology used to determine which DRAM architecture with FinFET technology is better is presented in the block diagram in Figure 3.

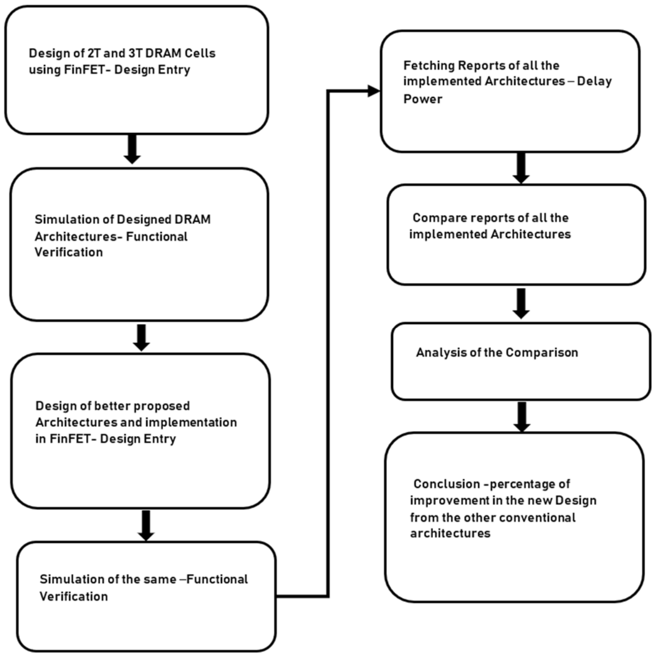

Fig. 3. Flowchart of the 2T and 3T DRAM design methodology.

Since 1T DRAM already exists and technology node scaling is coming from the industry, the area occupied by DRAM is already the smallest possible compared to SRAM. This paper focuses on reducing delay and power. Sleep transistors reduce leakage power in a circuit, and FinFET improves speed. Leakage power is the power lost due to a direct path between the Vdd and Gnd power rails in a circuit. To determine the percentage improvement in decreasing leakage power consumption or overall power consumption, the sleep transistor technique is employed, also considering speed. The time taken for read and write operations is observed and noted for comparison and conclusion. A sleep transistor is a high-VT pFET or nFET transistor that functions as a switch to cut power to sections of a design in holding mode. The pFET sleep transistor is referred to as a "header switch" because it switches the VDD supply. As portrayed in Figure 4, the nFET sleep transistor controls the ground supply and is therefore referred to as a "footer switch." The sleep approach reduces subthreshold leakage by isolating the gates from the power source and ground. In this method, the sleep transistor is used between the Gnd and the pull-down network, as well as between the power supply Vdd and the pull-up network. In idle mode, the sleep transistor cuts the circuit by turning off the power rails to minimize leakage power. M1 is the sleep transistor for the pull-up network, and M2 is the sleep transistor for the pull-down network. These two transistors protect the logic gate.

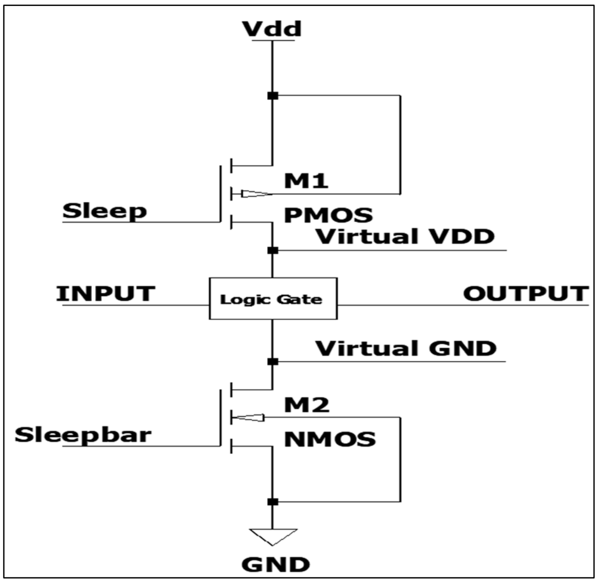

Fig. 4. Block diagram showing sleep transistor technique.

B. 2T-DRAM with Sleep Transistor

Figure 5 shows that the new FinFET 2T-DRAM is designed with two sleep transistors — one PMOS and one NMOS — receiving inverted inputs, which enables the entire circuitry to perform operations. The write transistor and the grounded capacitor are placed between the sleep transistors. The read transistor is placed near the read output, while the write and read inputs are given to the respective transistors. The inverted input for the sleep transistors is provided via a NOT gate.

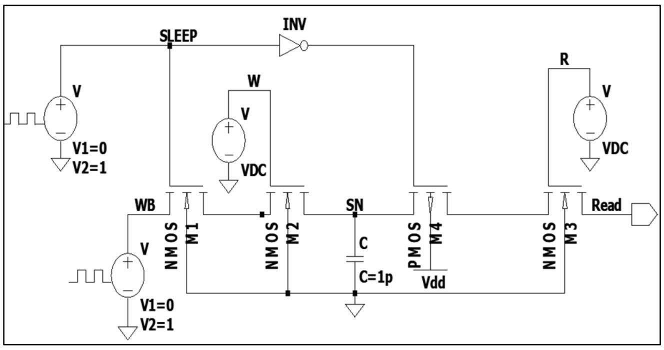

Fig. 5. Proposed 2T-DRAM with sleep Transistors.

The write operation only occurs when sleep is logic high. When W is high, WB is stored in the capacitor and when sleep and R are high and W is low, the charge stored in the capacitor is read. Figure 6 illustrates the schematics of the proposed 2T-DRAM array, built in Cadence, and the read and write plots were obtained. This 2T-DRAM is designed with a simple sleep transistor circuitry alternative to the access transistor. Once the sleep transistors are enabled, the main circuit is enabled for read and write operations, followed by the access transistor for operations. When the circuit is not in use, the sleep transistors are off, which prevents leakage power. To write a logic '1' or '0', W must be driven high and R must be driven low while WB is '1' or '0', respectively. The same value will be written in the storage capacitor. For a read operation, R is driven high while W is driven low. The value stored in the capacitor is read from the read output.

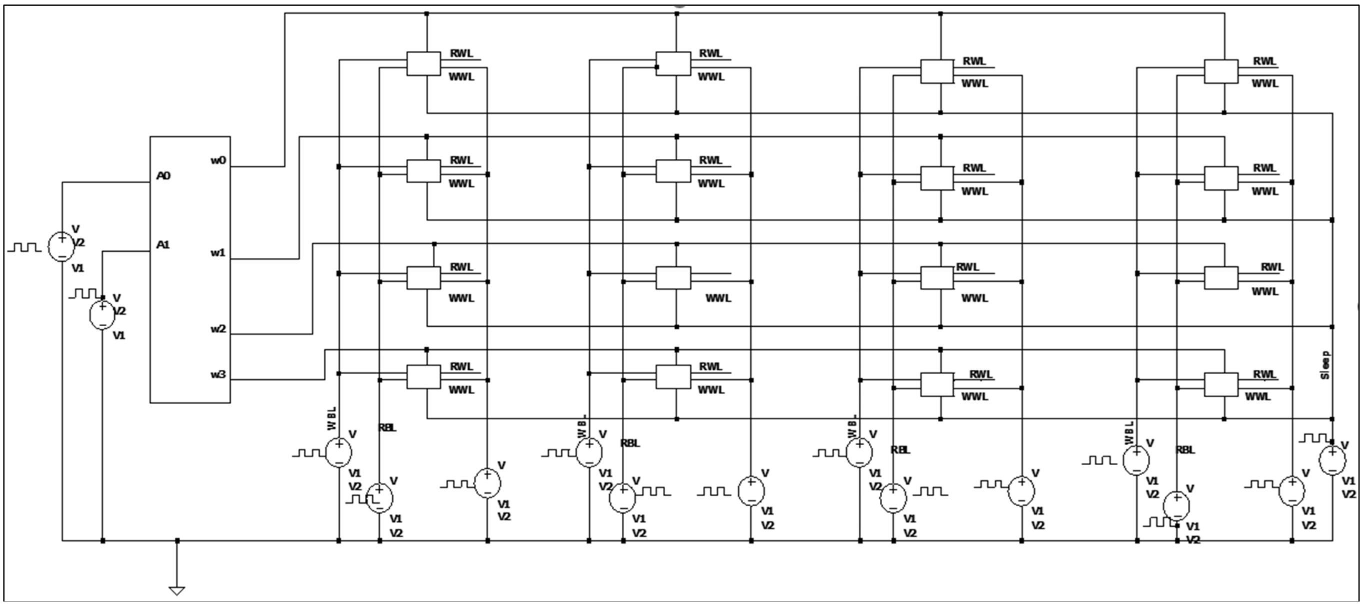

Fig. 6. Schematic of proposed 2T-DRAM 4X4 array with sleep transistors.

C. 3T-DRAM (B) with Sleep Transistor

The novel FinFET 3T-DRAM design uses two sleep transistors nMOS. Two capacitors store the write value, which stabilizes the current and improves the accuracy of the output reading. One transistor is placed between the grounded capacitors, whereas the center transistor is activated during both the write and read operations and turned off when the circuitry is not in use. The write transistor is located between the sleep transistors, and the read transistor is connected to the read line. Figure 7 displays the circuit diagram of the proposed 3T-DRAM(B) with sleep transistors.

For the write operation, the sleep and W lines must be at a logic high. For a read operation, the sleep and R must be logic high, and the stored value in the capacitor is read. Figure 8 presents the schematic of the proposed 3T-DRAM(B) array, with a sleep transistor designed with two sleep transistors that have the same input. The sleep transistors enable the main circuitry for read and write operations. Next, the access transistor must be enabled for operations. When the circuit is not in use, the sleep transistors are off, which prevents leakage power. The center transistor is also enabled by setting N to 1 throughout the operations. To write a logic '1' or '0', W must be driven high and R must be driven low while WB is '1' or '0', respectively. The same value will be written in the storage capacitors. For a read operation, R is driven high while W is driven low. The value stored in the capacitors discharges through the read capacitor and is read at the output terminal.

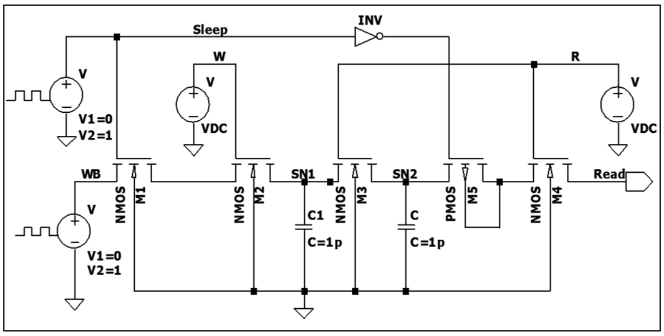

Fig. 7. Proposed 3T-DRAM (B) with two sleep transistors.

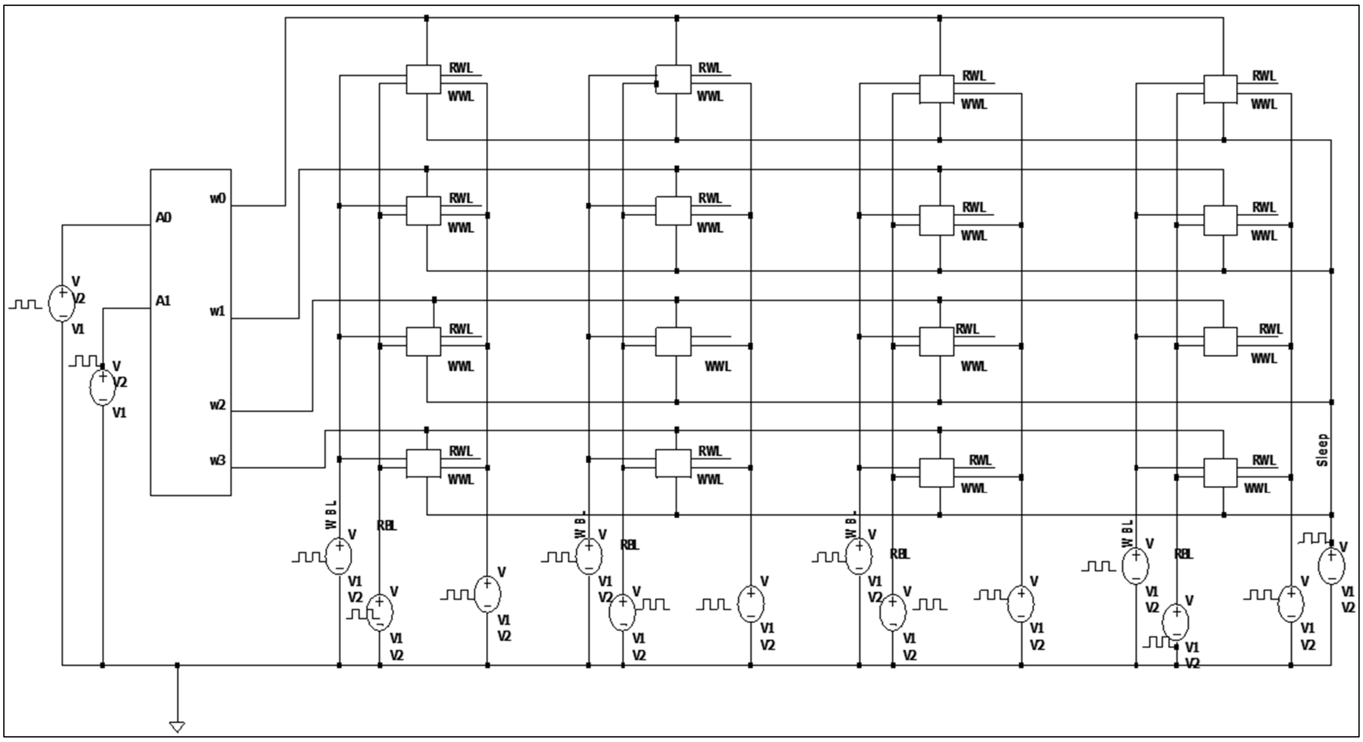

Fig. 8. Schematic of proposed 3T-DRAM(B) 4X4 Array with sleep transistors.

D. 3T-DRAM (C) with Sleep Transistors

This 3T-DRAM contains 3 transistors. One pMOS transistor on the write line and five nMOS transistors and/along with a capacitor that stores the write value and is connected to the center of the circuit. The capacitor's ground is connected through the nMOS transistors, so unlike previous circuits, the sleep transistor is given '0' for the write operation and '1' for the read operation. The circuit diagram of the proposed 3T-DRAM(C) with sleep transistors is shown in Figure 9. For the write operation, the sleep and W lines are logic high, and the value on the WB line is stored in the capacitor. For the read operation, the sleep and R must be logic high, while W must be logic low. Then, the stored value is read through the output pin. Figure 10 depicts the schematic of the proposed 3T-DRAM(C) array.

This 3T-DRAM with sleep transistors is designed using three sleep transistors with the same input. During the write operation, the pMOS sleep transistor is enabled, while the nMOS sleep transistors are disabled when the gate of the sleep transistors is driven to '0'. W is made high, and R is made low. The WB value is stored in the storage capacitor. For the read operation, the p-channel sleep transistor is disabled and the n-channel sleep transistors are enabled when the gate of the sleep transistors is driven to '1'. W is made low, and R is made high. The stored WB value discharges through the read transistor and is read at the output terminal. DRAM cells with 4T or more were not given much attention during the selection process because SRAM cells with 4T or more are available and preferred. However, 3T DRAMs were examined because a single circuit can be used for both writing and reading without interruption.

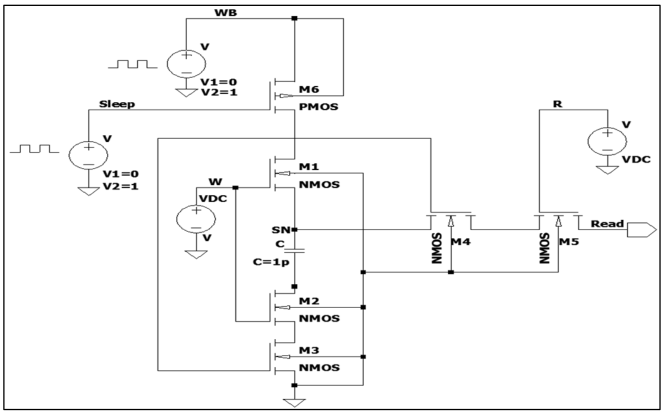

Fig. 9. Proposed 3T-DRAM(C) with three sleep transistors.

III. RESULTS AND DISCUSSION

Different DRAM designs, including conventional and the proposed architectures with sleep transistor configurations, were created. These structures were built using the FinFET technology library for 18 nm in Cadence Virtuoso. The DRAM designs were also simulated and verified in the ADE environment offered by the Cadence Virtuoso tool. Table I outlines the delays and percentages of improvement from the existing conventional architectures to the new proposed architectures of the cells and arrays, while Table II provides power details for single cell DRAMs, for both existing and proposed architectures. Table III shows the power results obtained for the arrays. The tables/ Tables I- III provide data on which architectures optimize delay and consume power during read and write operations. In almost all power reports concerning sleep transistor configurations, sleep signals allow the circuits to be active only half the time they are simulated. The percentage decrease in power consumption when using the proposed novel architectures compared to conventional circuits is also shown, together with the delay and power reports for existing DRAM circuits and the proposed novel circuits. As verified, the delay is improved by 66% for the write operation and 98% for the read operation. The novel proposed designs are compared to their conventional counterparts. The novel 2T-DRAM with sleep transistor circuit offers a 56.8% power reduction during write operations and up to a 99.8% power reduction during read operations compared to its conventional counterpart.

Similarly, the proposed 3T-DRAM(B) with sleep transistors offers a power reduction of 63.02% during write operations and up to 99.5% during read operations compared to its conventional counterpart. The proposed novel 3T-DRAM(C) cell with sleep transistors offers up to 99.6% power reduction during the write operation and up to 99.8% power reduction during the read operation compared to its conventional counterpart. Thus, the novel 3T-DRAM(C) design is proven to provide improved delay for read operations and maximum power savings compared to the others. Next are the 2T-DRAM and 3T-DRAM(B), which are superior to conventional 3T-DRAM.

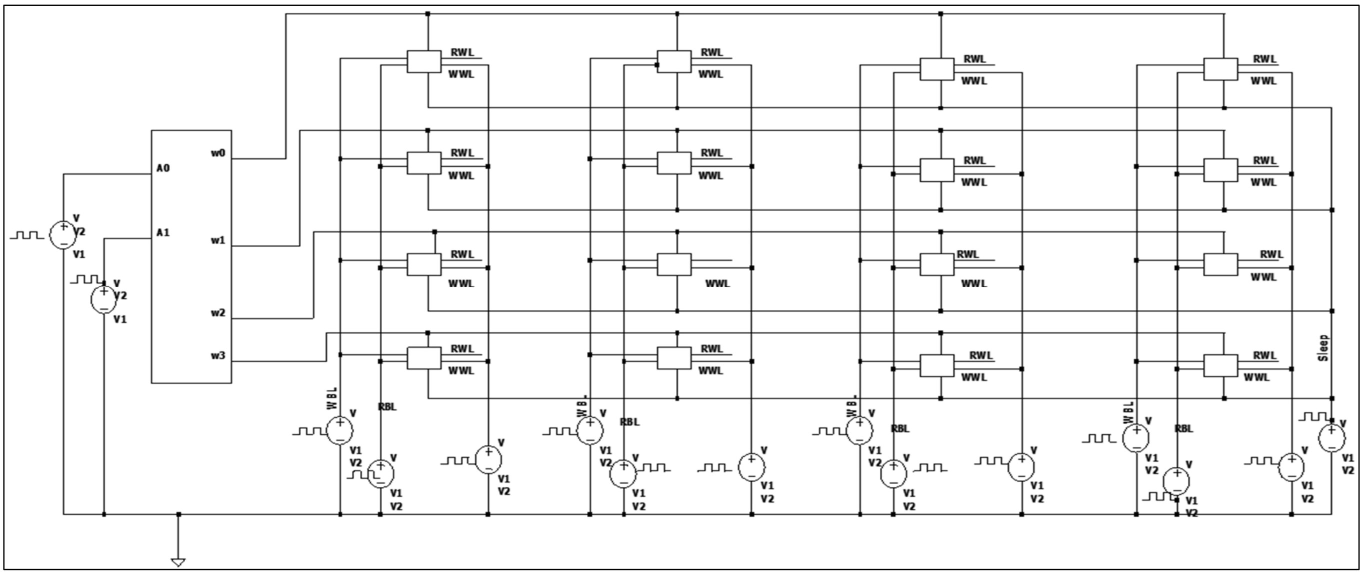

Fig. 10. Schematic of proposed 3T-DRAM(C) 4X4 array with sleep transistors.

TABLE I. COMPARISON OF DELAY IN CELLS AND ARRAY

DRAM design			Delay (nsec)		Percentage of improvement (%) (w.r.t. conventional)	
			Write	Read	Write	Read
Cell	2T	Conventional	38.09	0.012796	66	59.58
		Proposed with sleep transistors	12.95	0.02042		
	3T	Conventional	6.432	0.09242	1.66	0.34
		Proposed(B) with sleep transistors	6.539	0.09273		
		Proposed(C) with sleep transistors	19.97	0.001838	210.5	-0.98
Array	2T	Conventional	51.02	24.73	79	319
		Proposed with sleep transistors	10.66	103.6		
	3T	Conventional	11.41	18.66	0.54	8.04
		Proposed(B) with sleep transistors	11.472	20.16		
		Proposed(C) with sleep transistors	33.21	12.79	191.06	31.46

TABLE II. COMPARISON OF POWER CONSUMPTION IN CELLS

DRAM Cells		Power consumption (nW)		Percentage of improvement (%) (w.r.t. conventiona)	
		Write	Read	Write	Read
2T	Conventional	14920	16860	56.8	99.8
	Proposed with sleep transistors	6432	31.48		
3T	Conventional	17410	6310	63.02	99.5
	Proposed(B) with sleep transistors	6437	31.48		
	Proposed (C) with sleep transistors	68.74	11.11	99.6	99.8

TABLE III. COMPARISON OF POWER CONSUMPTION IN ARRAYS

DRAM Arrays		Power consumption (in W)		Percentage of improvement (%)(w.r.t. conventional)	
		Write	Read	Write	Read
2T	Conventional	5.591m	752.6m	99.99	15.57
	Proposed with sleep transistors	10.66n	635.4m		
3T	Conventional	672m	21.164m	54.2	98.6
	Proposed (B) with sleep transistors	307.9m	296.3m		
	Proposed (C) with sleep transistors	216.4m	95.36m	67.78	99.55

IV. CONCLUSIONS

The Cadence Virtuoso tool was used to design Dynamic Random-Access Memory (DRAMs) with conventional and proposed architectures, both of which use FinFETs with sleep transistor configurations, using the analog design environment in order to simulate these configurations. A comparison was carried out between conventional FinFET DRAM architectures and proposed FinFET DRAM architectures using the sleep transistor technique. The output waveforms were examined for operational accuracy, and the voltage levels were measured. Using the data from Tables I-III, engineers can determine which proposed circuit to select based on the design requirements. There is clearly an improvement in speed or reduction in delay in two cases: the write operation of the novel proposed 2T DRAM with sleep transistors compared to the conventional one and the read operation of the novel proposed 3T DRAM (C) with sleep transistors compared to the conventional one. The other cases show an increase in delay. However, designers should consider this increase as a trade-off parameter depending on their system requirements. The new proposed 3T-DRAM(C) is proven to provide the greatest power savings compared to the others, followed by the 2T-DRAM and the 3T-DRAM(B), which are superior to conventional 3T-DRAM. Ultimately, the designer must consider the system design requirements and specifications to select the proposed cells and 4x4 array structure. The sleep transistor technique provides maximum power savings and improves scalability by reducing leakage during idle periods. Sleep mode slows the discharge of the internal storage node, resulting in a longer retention time and a reduced refresh frequency, while FinFETs help increase speed, solving the problem of DRAM memory. This concept can be extended to study how cells behave when configured in large array structures. Such a study will expand a designer's understanding of the advantages and disadvantages of using these cells in an array. Further examination can compare the proposed designs with emerging non-volatile memories, such as STT-RAM and RRAM. The aim is to develop optimized hybrid architectures for low-power, high-performance computing systems.

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