Design and Test of a New Three-Phase Multilevel Inverter for PV System Applications

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***Abstract*—This paper presents a test of a new three-phase multilevel inverter for PV system applications with reduced number of used DC sources and power switches. The topology of the inverter is designed using an electric assemblage of a two-level dc-dc boost converter (TLBC) with a simplified three-phase multilevel DC-AC converter (THPMC). The TLBC generates two balanced output DC voltages, while the THPMC converts these two DC voltages and generates three-phase AC voltages with five levels per line. Two modulation control techniques are used and tested with the proposed PV system on PSIM and on ISIS Proteus software. The achieved results prove the simplicity and efficiency of the proposed three-phase inverter.**

Keywords-PV; boost converter; multilevel inverter; three-phase inverter; SPWM; microcontroller

I. INTRODUCTION

Multilevel inverters offer the possibility of increasing the efficiency of the PV energy conversion chain. They deliver optimal AC voltages and currents with fewer harmonics (low THD), reduce voltage transients across industrial machines windings, present low electromagnetic interference, make low switching losses across power switches, and use small filters [1-4]. Their basic structures are arranged in three categories: neutral point clamped inverter, cascaded H-bridge inverter, and flying capacitor. Currently, various configurations are developed in different arrangements such as symmetric, asymmetric and hybrid topologies [5-7]. In the case of three-phase versions, several structures have been discussed depending on the number of used DC sources, power switches, and the complexity of the design and control scheme [8, 9]. This paper exposes the test of a new three-phase multilevel inverter, which delivers AC voltages with five levels per line. The associated DC-AC converter requires two voltage sources at the DC-Bus. It is simplified from [10] where four DC sources have been used to get the same levels. The structure of the multilevel inverter is established from the single-phase inverters presented in [2, 11, 12]. In this study, the two voltage sources are obtained from an efficient multilevel DC-DC boost converter tied to solar panels. The proposed PV system is tested on PSIM software with high switching frequency modulation technique and on ISIS Proteus software with a fundamental switching method programmed on a model of a low-cost microcontroller.

II. DESCRIPTION OF THE PROPOSED INVERTER

Figure 1 shows the topology of the proposed three-phase multilevel inverter. It includes one single DC source from solar panels (Vin), a two-level DC-DC boost converter (TLBC), and a three-phase multilevel DC-AC converter (THPMC).

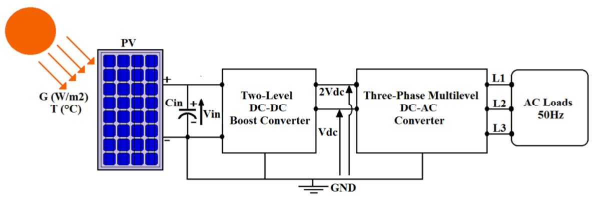

Fig. 1. Topology of the proposed three-phase multilevel inverter.

A. Solar Panels

Solar panels contain an association of small solar cells, which produce DC current when exposed to sunlight (photons). There are several types of solar cells such as mono-crystalline, polycrystalline and multi-junction. Figure 2 shows a model of a solar cell composed of a current source, a single diode, a series resistance, and a parallel resistance [2, 13]. In Figure 2:

$$I = Iph - Id - Ish =$$

$$Iph - I_0\left[\exp\left(q \times \left(\frac{V+(Rs\times I)}{n\times K\times T}\right)\right) - 1\right] - \frac{V+(Rs\times I)}{Rp} \quad (1)$$

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where, Iph is the photocurrent, I is the output current, I_0 is the reverse saturation current of the diode, q is the electron charge (1.602×10^{-19}C), K is the Boltzmann constant (1.381×10^{-23}J/K), V is the output voltage, n is the ideality factor of the diode, and T is the junction temperature in Kelvin. Table I indicates the electrical parameters of the used solar panels under standard test conditions (STC) (1000W/m^2, 25°C).

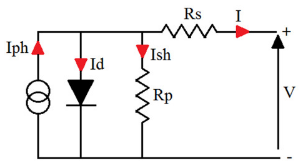

Fig. 2. Model of a solar cell

TABLE I. SOLAR PANEL PARAMETERS (STC)

Parameters	Values
Maximum power (Pmax)	240W
Voltage at Pmax (Vmp)	29.9V
Current at Pmax (Imp)	8.03A
Short-circuit current (Isc)	8.60A
Open-circuit voltage (Voc)	37.0V

B. Two-Level DC-DC Boost Converter

The used TLBC is shown in Figure 3. It's a non-isolated DC-DC converter composed of one inductor, one power switch, three diodes, and three capacitors. It's used to step-up the input voltage Vin in order to deliver two balanced output voltages (Vdc and 2Vdc) [14, 15].

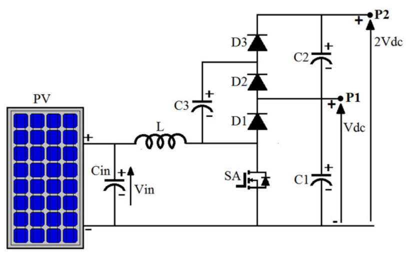

Fig. 3. The structure of the TLBC.

$$\mathrm{VP1} = \mathrm{Vdc} = \frac{\mathrm{Vin}}{(1-\mathrm{D})} \quad (2)$$

$$\mathrm{VP2} = 2\mathrm{Vdc} = \frac{2\times\mathrm{Vin}}{(1-\mathrm{D})} \quad (3)$$

where D is the duty cycle of the PWM control signal of the power switch SA.

C. The Proposed Three-Phase Multilevel DC-AC Converter

The generalized structure of the proposed new THPMC is shown in Figure 4. It consists of a simple three-phase bridge composed of 6 switches (SAH, SAL, SBH, SBL, SCH, SCL) without assembling the drains of the high side, three blocks of parallel power switches [(Q1, Q2, QA1,…., QAn-2), (Q3, Q4, QB1,…., QBn-2), and (Q5, Q6, QC1,…., QCn-2)] connected to the high side of the three-phase bridge through the power switches (SAH, SBH, SCH) and a block of DC voltage sources.

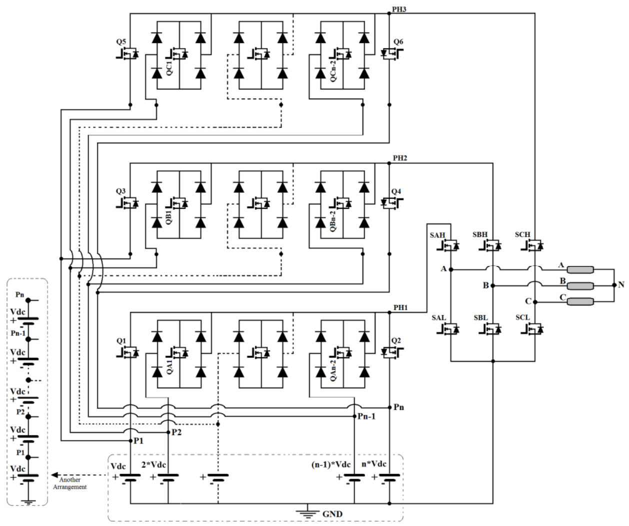

Fig. 4. Generalized circuit of the proposed THPMC

This multilevel DC-AC converter is easy to tie with batteries, solar panels, and DC-DC converters, because all used DC voltage sources have a common line to the ground (GND). The operation of the THPMC is based on controlling each power switch from the three blocks of parallel power switches with complementary pulses to get a positive staircase voltages at the points PH1, PH2, and PH3, while the three-phase bridge is used to inverse the polarity of these voltages and add the state zero to get three-phase AC voltages with a desired frequency (50Hz in this paper). Figure 5 shows the generalized staircase voltage at the point PH1. Figures 6 and 7 show the derived structures to get five levels per line (THPMC-5L) and seven levels per line (THPMC-7L) respectively. The studied structure in this paper is the THPMC-5L. Table II resumes the operation modes of this converter, while Figure 8 shows the waveforms of the obtained voltages per line.

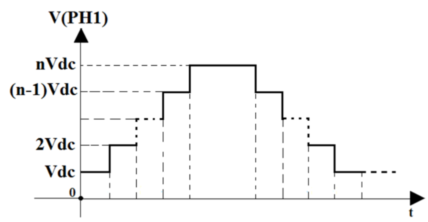

Fig. 5. Generalized staircase voltage at PH1

III. MODULATION ALGORITHM OF THE THPMC-5L

The gate pulses of the THPMC-5L are obtained by using an efficient sinusoidal pulse-width modulation method (SPWM). The latter is based on comparing two identical triangular carrier signals (Carr1 and Carr2) (having a DC offset equal to their amplitudes) with a reference sinusoidal signal (Ref), as shown in Figure 9 [10, 16]. Table III shows the used conditions to activate the power switches [Q1, Q2, SAH, and SAL] with the SPWM method. For the other blocks of power switches ([Q3, Q4, SBH, SBL], and [Q5, Q6, SCH, SCL]), their gate pulses are obtained by shifting just the reference signal with -120° and 120° respectively.

TABLE II. SWITCHING PATTERNS OF THE THPMC-5L WITH THE OPERATION MODES

Modes	Q1	Q2	SAH	SAL	Q3	Q4	SBH	SBL	Q5	Q6	SCH	SCL	VAB	VBC	VCA
M1	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	0	2Vdc	-2Vdc
M2	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	Vdc	Vdc	-2Vdc
M3	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	2Vdc	0	-2Vdc
M4	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	2Vdc	-Vdc	-Vdc
M5	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	2Vdc	-2Vdc	0
M6	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	Vdc	-2Vdc	Vdc
M7	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	0	-2Vdc	2Vdc
M8	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	-Vdc	-Vdc	2Vdc
M9	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	-2Vdc	0	2Vdc
M10	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF	-2Vdc	Vdc	Vdc
M11	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	-2Vdc	2Vdc	0
M12	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	-Vdc	2Vdc	-Vdc

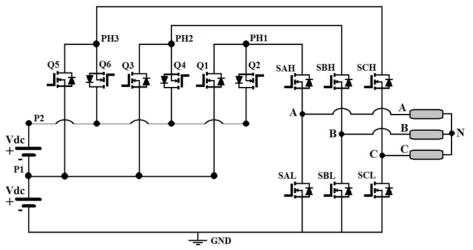

Fig. 6. The structure of the new THPMC-5L.

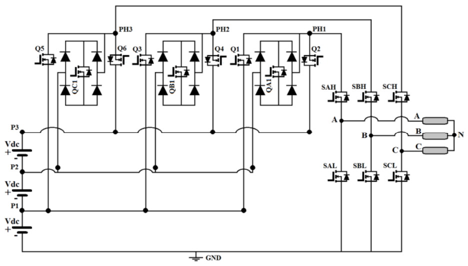

Fig. 7. The structure of the new THPMC-7L.

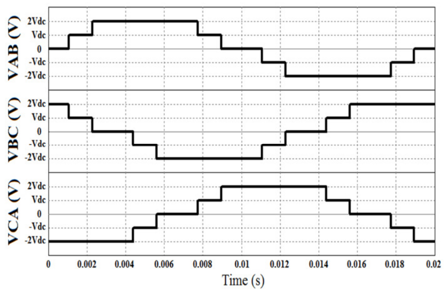

Fig. 8. Waveforms of the obtained voltages per line (THPMC-5L)

IV. SIMULATION ON PSIM

The proposed THPMC-5L associated with the TLBC as described in Figure 1 is tested on PSIM. Two identical solar panels (Table I) coupled in series are used as a DC source (Vin) under STC conditions. TLBC is controlled with a PWM signal (Fs=31KHz, D=0.55), while SPWM is implemented with a modulation index of 0.9 and a switching frequency of 5KHz. All output loads are coupled in Y connection with equal impedances (R=55.44Ω, L=0.14H). Figures 10 to 15 show respectively the input voltage (Vin) and input current (Iin) from solar panels, the output voltages from the TLBC, the output AC voltages per line, the output AC voltages per phase, the output AC currents per phase, and the FFT analysis of the AC voltages per line.

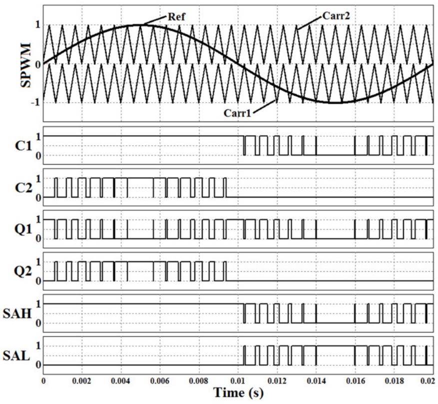

Fig. 9. SPWM method with the generated gate pulses for one leg of the THPMC-5L.

TABLE III. USED SIGNALS AND LOGICAL CONDITIONS TO ACTIVATE THE POWER SWITCHES FOR ONE LEG OF THE THPMC-5L

Signals/Conditions	ON switch
(Ref ≥ Carr1) = C1	SAH
(Ref ≥ Carr2) = C2	Q2
{C1 AND (NOT C2)}	Q1
(NOT C1)	SAL

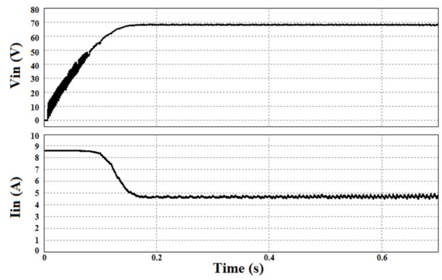

Fig. 10. Input voltage (Vin) and input current (Iin) from solar panels.

The two solar panels deliver an input voltage Vin of 68.38V and an input current Iin of 4.72A. The TLBC subjected to the input voltage supplies two balanced output voltages

(VP1=154.65V, VP2=309.24V) to the THPMC-5L which delivers three-phase AC voltages (50Hz) with five levels per line (182V RMS) and nine levels per phase (105V RMS), while the output AC currents per phase are in sinusoidal form (1.38A RMS). The FFT spectrum shows that the inverter generates very few harmonics without using filters.

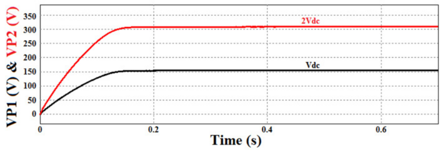

Fig. 11. Output voltages from the TLBC.

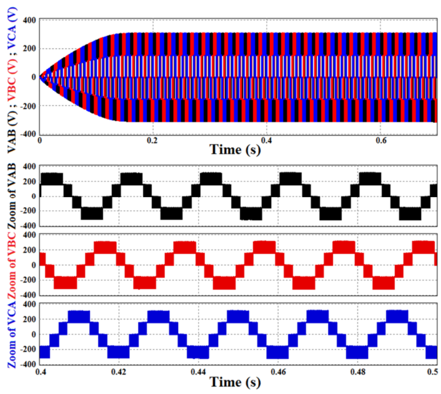

Fig. 12. Output AC voltages per line (VAB, VBC, and VCA) with SPWM method.

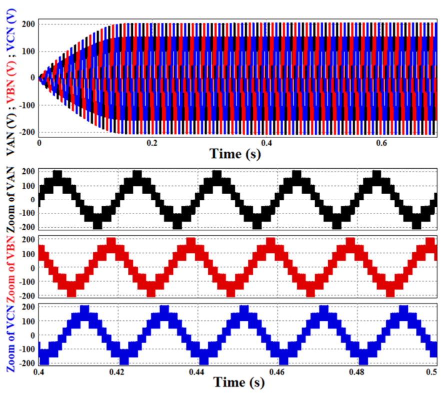

Fig. 13. Output AC voltages per phase (VAN, VBN, and VCN) with SPWM method.

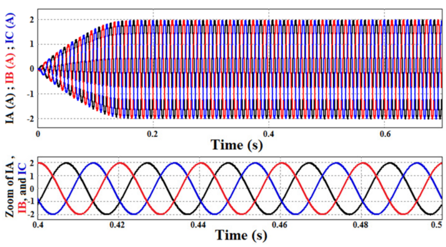

Fig. 14. Output AC currents per phase (IA, IB, and IC) with SPWM method.

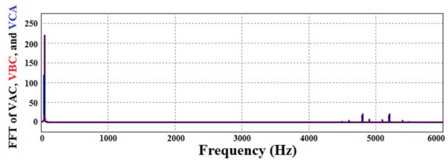

Fig. 15. FFT spectrum of the output AC voltages per line with SPWM method.

V. IMPLEMENTATION ON ISIS PROTEUS

The operation of the studied THPMC-5L is also verified on ISIS Proteus with fundamental switching method. For this, a test code has been written and uploaded into a model of a microcontroller (Arduino-Uno) based on the suggested switching states in Table II. Figure 16 shows the synoptic of the test bench developed on ISIS Proteus.

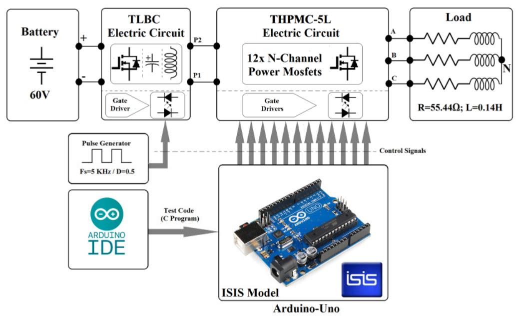

Fig. 16. Synoptic of the test bench on ISIS Proteus.

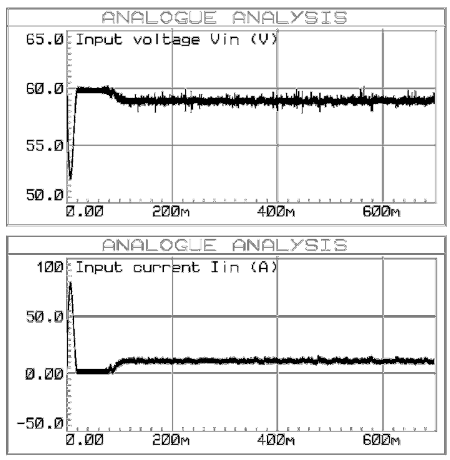

Fig. 17. Input voltage (Vin) and input current (Iin) from the battery.

Figures 17 to 21 present respectively the input voltage (Vin) and input current (Iin) from the used battery, the output voltages from the TLBC, the output AC voltages per line, the output AC voltages per phase, and the output AC currents per phase. From these results, the used battery delivers an input voltage Vin of 59V and an input current Iin of 11.3A. The TLBC supplies two balanced output voltages (VP1=151V, VP2=300V) to the THPMC-5L. The latter delivers AC voltages (50Hz) with five levels per line and seven levels per phase. Also, the output AC currents per phase are similar to a sinusoidal in shape without using filters.

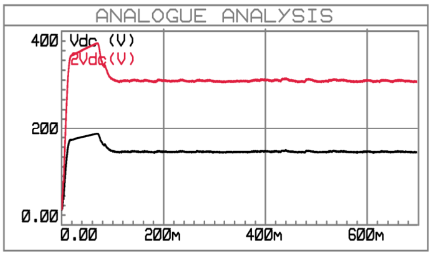

Fig. 18. Output voltages from the TLBC.

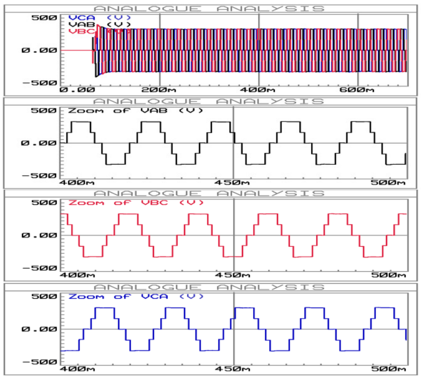

Fig. 19. Output AC voltages per line (VAB, VBC, and VCA) with fundamental switching method.

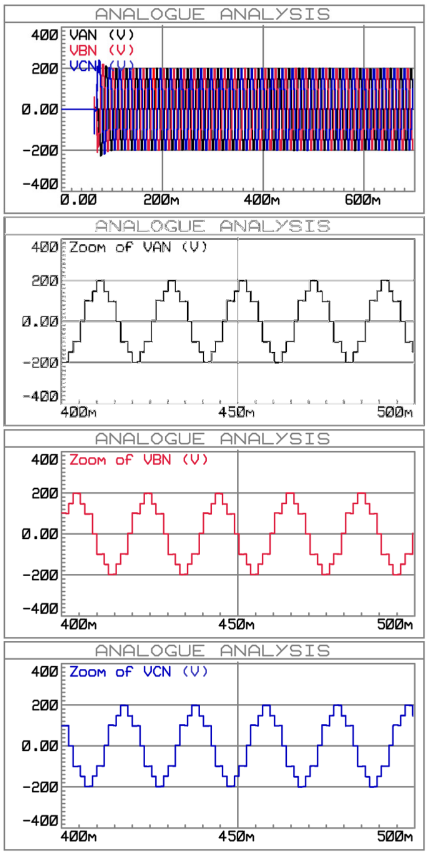

Fig. 20. Output AC voltages per phase (VAN, VBN, and VCN) with fundamental switching method.

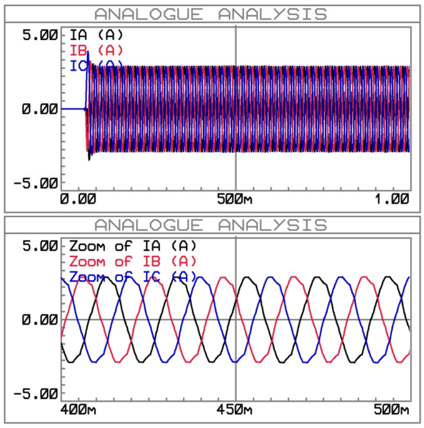

Fig. 21. Output currents per phase (IA, IB, and IC) with fundamental switching method.

VI. Conclusion

In this paper, a test of a new simplified three phase multilevel inverter has been presented. To generate three-phase AC voltages with five levels per line, the proposed inverter requires just twelve power switches and two voltage sources for the DC-AC converter. The latter can be tied directly with batteries and solar panels or with DC-DC converters such as the studied two-level boost converter. Two different modulation techniques have been tested. The first one depends on high switching frequency which has been tested on PSIM, and the second one depends on low switching method evaluated with a C program uploaded on a model of a microcontroller which was tested on ISIS software. The proposed inverter is able to be tied with solar panels and deliver optimal AC voltages and currents with low THD without causing voltage balancing problems across the used capacitors. The suggested applications of this inverter are PV pumping systems and energy injection into the grid. The future scope of this work is the experimental implementation of the full PV system with a closed loop control system on a DSP card.

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