

# Performance Investigation of Different Topologies of 1-100 GHz on-chip Transformers using 130 nm SiGe BiCMOS

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**Abstract**—In this study, modeling and designing different topologies of on-chip transformers are presented using 130nm SiGe BiCMOS technology. Interleaved, stacked, and full symmetrical interleaved transformers are investigated. Octagon and square shapes are used for designing transformers with flipped and non-flipped feed lines. A comparison between performances of various configurations is presented using a full-wave simulator. The octagon stacked transformer with flipped feed lines showed a good performance at around 60GHz. The simulated results demonstrated a coupling factor  $K$  of 0.94, minimum insertion loss of 1.01518dB, and Q-factor of 9 with a minimum occupied area of 0.0019mm<sup>2</sup>.

**Keywords**—on-chip transformer; 130nm SiGe BiCMOS technology; interleaved transformer; stacked transformer

## I. INTRODUCTION

The growing demand for high quality and high data rate in a wireless telecommunication system increases the challenge for designing high performance electronics components. Particularly for a high frequency bands applications [1, 2], the substrate losses in passive devices have become dominant due to the proximity and skin effect [3, 4]. On-chip transformer (TF) is one of the passive components for designing system-on-chip (SoC) applications. On-chip TF has been commonly used as a power splitter/combiner, and inter-stage impedance matching in many components design such as power amplifiers [5-7], low noise amplifiers [8, 9], mixers [10], and voltage controlled oscillators [11-13]. The TF is better to be compact, low loss, with high quality factor, easy impedance matching, and with the ability of conversion from differential to single ended for power combining as well as conversion from single ended to differential for power splitting [14]. Many researches have been conducted in modeling and designing of the on-chip TF. The elements of the device can be extracted from the geometrical shape and technological data of the transformer [15]. However, this model is compatible up to 10GHz. Other broadband models for millimeter-wave TF working up to

100GHz, and 110GHz have been proposed in [16, 17]. Moreover, an on-chip six ports TF model was reported in [18].

In this paper, a simple model based on lumped elements of TF is presented. In addition, direct parameters extraction based on EM S-parameters simulation is used for design and simulation of different topologies of on-chip transformer. IHP 130nm SiGe BiCMOS technology is considered in this study in the frequency range between 1–100GHz.

## II. APPROACHES OF MODELING ON-CHIP TRANSFORMER

A transformer consists of two inductors for the primary and secondary windings. There are two approaches for extracting the parameters of these windings. The first method is using equivalent lumped components, while the second is direct parameter extraction from S-parameters using the EM Sonnet simulator. Figure 1 shows the equivalent circuit for the on-chip TF. The primary inductor has two ports, P1 and P2, the equivalent circuit model consists of six elements, three series elements represented by series capacitance  $C_p$ , inductance  $L_p$ , resistance  $R_p$ , as well as three substrate elements represented by oxide capacitance  $C_{p-ox}$ , substrate capacitance  $C_{p\_sub}$ , and substrate resistance  $R_{p\_sub}$ . The same elements have also been considered for the secondary inductor with two ports S1, and S2. Moreover,  $C_{ps}$  represents the mutual capacitance between the two windings. The values for the six elements of the lumped equivalent circuit shown in Figure 2 can be calculated based on the dimensions of the inductor. The series inductor  $L_p$  (nH) as a function of width  $w$  ( $\mu\text{m}$ ), length  $l$  ( $\mu\text{m}$ ), and thickness  $t$  ( $\mu\text{m}$ ) can be calculated as [16]:

$$L_p = \frac{0.42 \times \mu_0}{\pi} \cdot l \cdot \left[ \ln \left( \frac{2 \times l}{0.2235(w+t)} \right) + \frac{0.2235(w+t)}{l} - 1 \right] \quad (1)$$

Figure 2 shows the relationship between inductance (pH) and length of inductor ( $\mu\text{m}$ ) with variable width ( $\mu\text{m}$ ) of inductor and constant thickness ( $3\mu\text{m}$ ). It can be observed that, a smaller inductor width provides higher inductance. However, the width is constrained by the minimum width provided by the foundry.

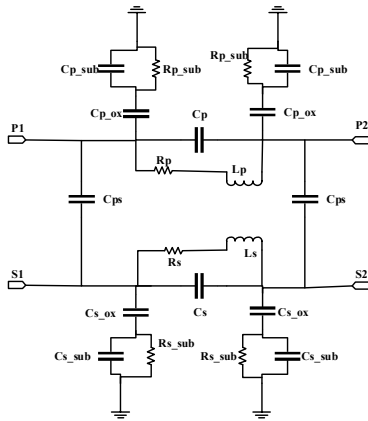


Fig. 1. Equivalent circuit of the on-chip transformer

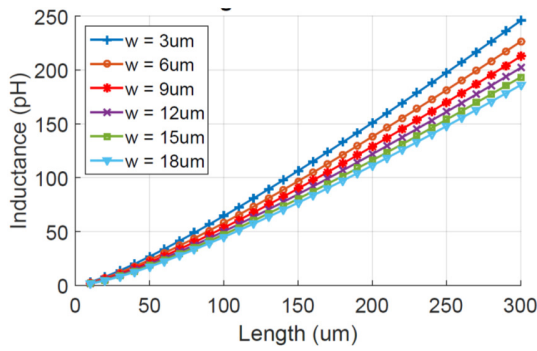


Fig. 2. Inductance values versus corresponding length with variable width and constant thickness=3um

The rest of the parameters for the primary and secondary inductors can be calculated using the following formulas [19]:

$$R_{series} \cong \frac{1}{w \times \sigma \times \delta (1 - e^{-t/\delta})} \quad (2)$$

$$\delta = \sqrt{\frac{2}{2\pi f \mu_0 \sigma}} \quad (3)$$

$$C_{series} = \frac{n \times w^2 \times \epsilon_{ox}}{t_{ox}} \quad (4)$$

$$C_{ox} = \frac{0.5 \times w \times l \times \epsilon_{ox}}{t_{ox}} \quad (5)$$

$$C_{sub} = 0.5 \times w \times l \times C_{si} \quad (6)$$

$$R_{sub} = \frac{2}{w \times l \times G_{si}} \quad (7)$$

where,  $\delta$ ,  $\sigma$ ,  $\epsilon_{ox}$ ,  $t_{ox}$  are skin depth, conductivity, permittivity, and thickness of the oxide layer respectively, while  $G_{si}$  and  $C_{si}$  represent conductance and capacitance respectively for the silicon substrate ( $C_{si} \cong 10^{-2} fF/um^2$ ,  $G_{si} = 10^{-7} S/um^2$ ).

Another approach for extracting parameters of the on-chip TF is using the 3D electromagnetic simulator (Sonnet) to generate the S-parameters. In that case, the following expressions are used for calculating primary inductance  $L_{pri}$ , secondary inductance  $L_{sec}$ , Q-factor for primary  $Q_{pri}$ , Q-factor for secondary  $Q_{sec}$ , and coupling coefficient K [20, 21]:

$$L_{pri}(pH) = \frac{Imag(Z_{11}) \times 10^{12}}{2\pi f} \quad (8)$$

$$L_{sec}(pH) = \frac{Imag(Z_{22}) \times 10^{12}}{2\pi f} \quad (9)$$

$$Q_{pri} = \frac{Imag(Z_{11})}{Real(Z_{11})} \quad (10)$$

$$Q_{sec} = \frac{Imag(Z_{22})}{Real(Z_{22})} \quad (11)$$

$$K = \sqrt{\frac{Imag(Z_{12}) \times Imag(Z_{21})}{Imag(Z_{11}) \times Imag(Z_{22})}} \quad (12)$$

Moreover, the parameters of differential configuration for the on-chip TF can be extracted using [22]:

$$Z_d = Z_{11} + Z_{22} - Z_{12} - Z_{21} \quad (13)$$

$$L_d = \frac{Imag(Z_d)}{2\pi f} \quad (14)$$

$$Q_d = \frac{Imag(Z_d)}{Real(Z_d)} \quad (15)$$

where,  $Z_d$ ,  $L_d$ , and  $Q_d$  are differential impedance, differential inductance, and differential Q-factor respectively.

### III. PERFORMANCE COMPARISON OF DIFFERENT TOPOLOGIES OF ON-CHIP TF DESIGN

Many topologies of the on-chip TF have been investigated. For stackup configuration top layers TM1 and TM2 were utilized to design primary and secondary windings. For the interleaved configuration TM2 layer was used for designing two windings, while TM1 layer was used for designing the secondary winding feed line. Figure 3 shows the eight different topologies of the on-chip TF considered in this study which are Octagon Interleaved TF with non-flipped feed lines (OITF)NF, Octagon Interleaved TF with flipped feed lines (OITF)F, Octagon Stacked TF with flipped feed lines (OSTF)F, Octagon Stacked TF with non-flipped feed lines (OSTF)NF, Square Interleaved TF with non-flipped feed lines (SITF)NF, Square Interleaved TF with flipped feed lines (SITF)F, Symmetric Square Interleaved TF (SSTF), and Symmetric Octagon Interleaved TF (SOTF). Single turn for both windings was utilized in all on-chip TF topologies because this approach provides low loss in high frequency operation. Table I shows the dimensions of on-hp transformer for all topologies.

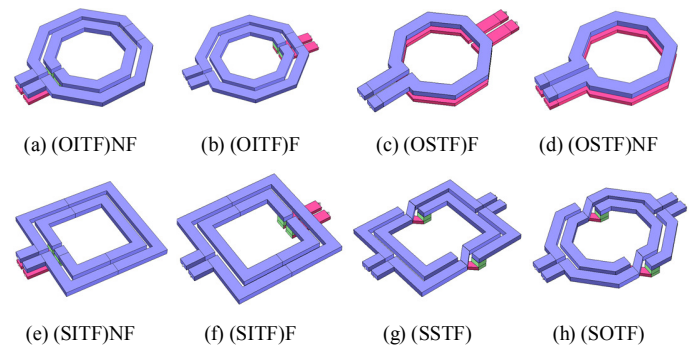


Fig. 3. Different topologies of the on-chip TF

TABLE I. DIMENSIONS OF ON-HP TRANSFORMERS

Transformer type	Wp $\mu\text{m}$	Ws $\mu\text{m}$	Dp $\mu\text{m}$	Ds $\mu\text{m}$	S $\mu\text{m}$	Area $\text{mm}^2$
Octagon Interleaved TF	5.45	5.45	58.97	43.87	2.1	0.0035
Octagon Stacked TF	5.45	5.45	43.87	43.87	2.1	0.0019
Square Interleaved TF	5.45	5.45	57.82	42.72	2.1	0.0033
Symmetric Square Interleaved TF	5.45	5.45	57.82	42.72	2.1	0.0038
Symmetric Octagon Interleaved TF	5.45	5.45	57.82	43.04	2.1	0.0038

This work addresses the effect of windings position on the performance of on-chip TF. Lateral and vertical magnetic couplings are available according to the position of windings on the stackup layers. Lateral magnetic coupling takes place in interleaved configuration when utilizing only one thick layer TM2 for the primary and secondary windings. On the other hand, vertical magnetic coupling takes place between windings as in stacked topology when utilizing two thick layers, TM1 and TM2. In addition, feed lines' direction has a significant effect on the performance of on-chip TF. To compare the performance of the proposed topologies shown in Figure 3, design and simulation of on-chip TF by using the Sonnet EM simulation has been carried out. Figure 4 shows the comparison of primary and secondary inductance for all proposed topologies of on-chip TF. It can be observed that all topologies provide high resonant frequency, greater than 100GHz. The flipped feed lines of all topologies have greater inductance than the non-flipped ones. However, the flipped feed lines have slightly reduced coupling between windings. Therefore, for selection between the two options of feed lines position, the minimum space layout for specific circuit design should be considered. Amongst all topologies of the on-chip TF the symmetric square interleaved TF shape has the greatest inductance for primary and secondary windings. Both (SSTF) and (SOTF) have the same inductance for their primary and secondary windings because of their high symmetrical shapes.

Figure 5 shows a comparison of Q-factor for all topologies. Both flipped and non-flipped feed line positions have been considered for simulation of the Q-factor of the primary and secondary windings. It can be seen that the transformers with flipped feed lines (represented by dash lines) have better values of Q-factor than the other transformers. The variation in primary and secondary values of Q-factor for the interleaved octagon and square shapes is due to the differences in their lengths of primary and secondary windings. However, the symmetric octagon and square transformers have almost the same values of Q-factors in their primary and secondary windings because they have full symmetrical shapes. Moreover, the octagon stacked transformers with flipped feed lines have better values of Q-factors than the one with non-flipped feed lines, which is because feed lines position in the same direction leads to imperfect coupling thus reducing quality factor.

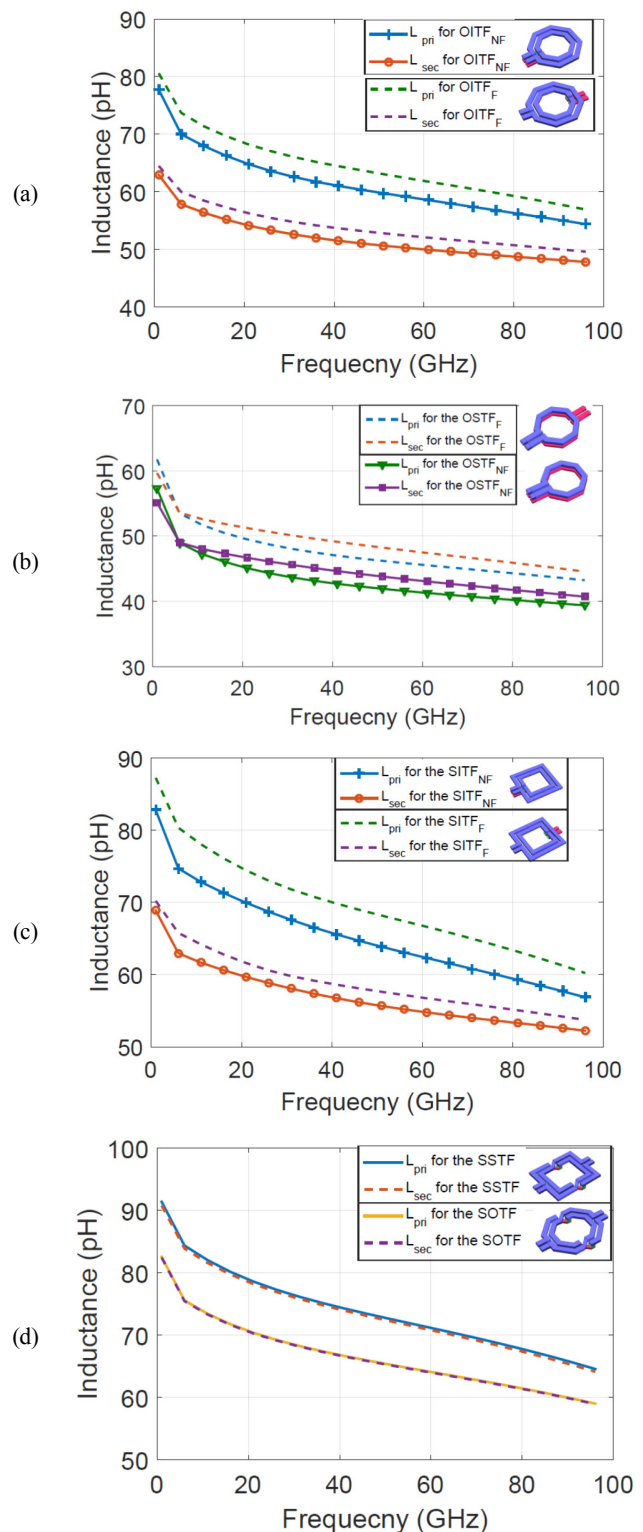


Fig. 4. Comparison of primary and secondary inductance for the different topologies of the on-chip TF, for the case of flipped (dash line) and non-flipped (solid line) feed lines. (a) Octagon interleaved TF (b) Octagon stacked TF (c) Square interleaved TF (d) Symmetrical square and octagon interleaved TF

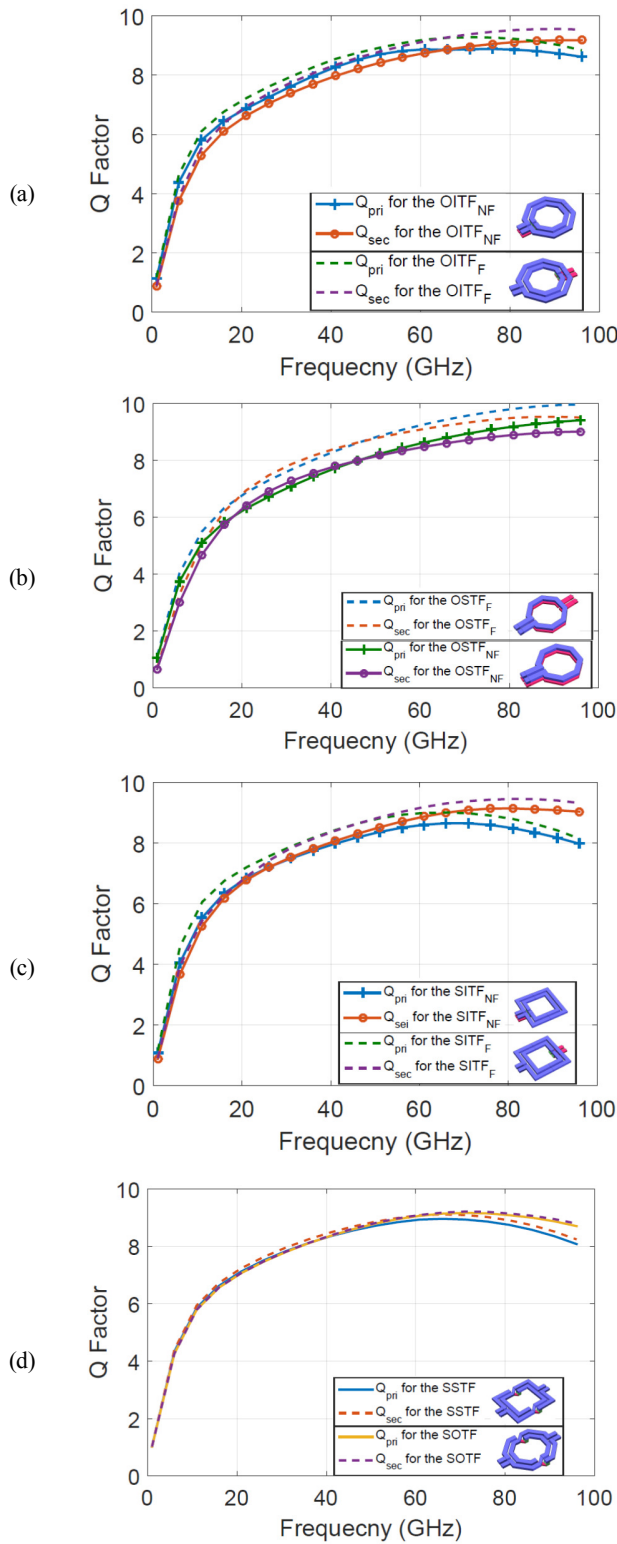


Fig. 5. Comparison of primary and secondary Q-factor for different topologies of the on-chip TF, for the case of flipped (dash line) and non-flipped (solid line) feed lines. (a) Octagon interleaved TF (b) Octagon stacked TF (c) Square interleaved TF (d) Symmetrical square and octagon interleaved TF

There are two approaches commonly used to find the figure-of-merit of TF. The first one is used when a TF is utilized in an application that requires high efficiency in power transmission. In this case the figure-of-merit can be calculated using maximum available gain  $G_{max}$ . [23, 24]:

$$G_{max} = \left| \frac{S_{21}}{S_{12}} \right| (k - \sqrt{k^2 - 1}) \quad (16)$$

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (17)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (18)$$

However, instead of using S-parameters, we can use Z-parameters:

$$G_{max} = 1 + 2(x - \sqrt{x^2 - 1}) \quad (19)$$

$$x = \frac{Re(Z_{11})Re(Z_{22}) - [Re(Z_{12})]^2}{[Im(Z_{12})]^2 + [Re(Z_{12})]^2} \quad (20)$$

The second method of determining the figure-of-merit of TF depends on the total loss of the device, using minimum insertion loss ( $IL_m$ ) expression [25]:

$$IL_m = \frac{1}{1 + 2(x - \sqrt{x^2 - 1})} \quad (21)$$

$$x = \frac{Re(Z_{11})Re(Z_{22}) - [Re(Z_{12})]^2}{[Im(Z_{12})]^2 + [Re(Z_{12})]^2} \quad (22)$$

On-chip TF has many sources of energy loss. Radiation loss takes place when dimension of the device is larger than the free space  $\lambda$ . Substrate coupling loss takes place according to capacitive coupling between substrate and conductor, therefore displacement current will leak into the substrate through lossy dielectric. In addition, ohmic losses (skin effect) as well as imperfect coupling between primary and secondary windings can be considered as a source of losses.

Figure 6 shows the simulated minimum insertion loss (dB), and coupling factor  $K$  for all on-chip TF topologies. At high frequencies insertion loss increases, while  $K$  decreases according to the effect of imperfect coupling between TF windings. As seen in Figure 6(a) the octagon stacked transforms have the lowest insertion loss compared to the rest of TF topologies, while the symmetrical square transformer has the largest values of insertion loss due to their larger winding size. Because of the largest value of insertion loss for the symmetrical square transformer, this topology of TF has a worst value of coupling factor  $K$  as shown in Figure 6(b), while the octagon stacked TF provides the best values of  $K$  amongst all topologies.

#### IV. CONCLUSION

A comprehensive study of on-chip transformer using 130nm SiGe technology has been presented. Different topologies, shapes, and feed line positions of transformers have been investigated, using the top thick metals TM1 and TM2 of the stackup layer technology. Two methods of calculating elements of primary and secondary windings were explored, which are use of the geometry of windings and direct element extraction from the S-parameters. 3D electromagnetic simulation was carried out and the performance of transformers was compared in terms of inductance, quality factor, coupling

factor, and minimum insertion loss. This study can present a guideline for designing on-chip transformer for purposes of power splitting and combining in applications like power amplifiers, voltage control oscillators, and mixtures.

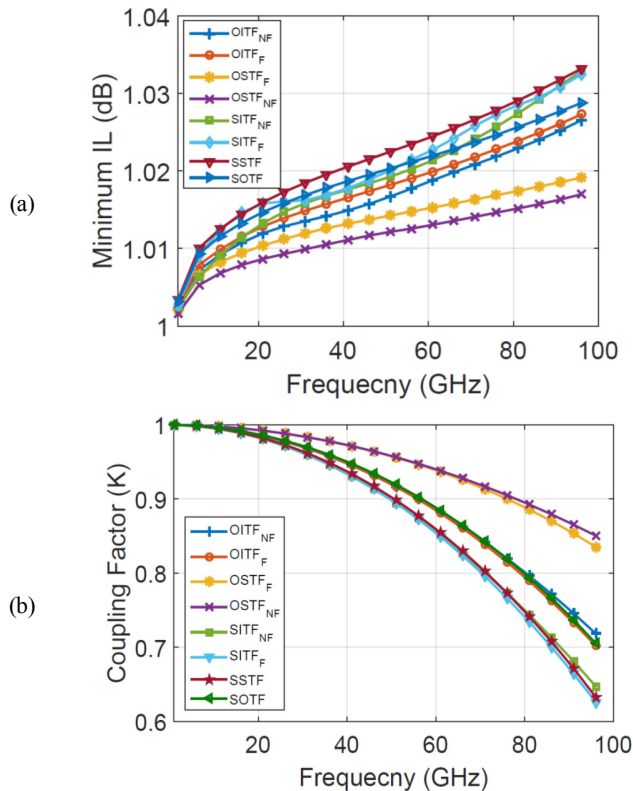


Fig. 6. Figure 6: Comparison values of (a) Minimum insertion loss, and (b) Coupling factor K for different topologies of the on-chip TF

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