Memristor, Memcapacitor, Meminductor: Models and Experimental Circuit Emulators

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Abstract-Before 1971, the number of passive electrical components was limited to three: resistor, capacitor, and inductor. In 1971, Pr. Chua predicted the existence of a fourth element, called memristor, since it corresponds to a resistor with memory behavior. Several years later, the concept of memory circuit was extended to capacitors and inductors. This paper proposes mathematical models for mem-elements, validated by Matlab and experimental circuit emulators for memcapacitor and meminductor. The experimental results show a good fit between theory, Ltspice simulations, and emulation circuits.

Keywords-memristor; memcapacitor; meminductor; models and simulations; experimental emulator

I. INTRODUCTION

The memristor, or memory resistor, is a two-terminal passive electronic component. Memristor, as a concept, was introduced in 1971 by Leon Chua [1]. Chua defined the behavior of the memristor by a constitutive relationship between flux and charge linkage. However, the concept of memristor did not catch the attention of the scientific community until 2008. The electronic community continued to develop analog and digital circuits without considering the tremendous potential of memristors [2-4]. In fact, Hewlett Packard (HP) Labs manufactured the first memristor component with layers of TiO_2 between two layers of Pt in 2008 [5]. HP also introduced a mathematical model of component operation. The scientific community criticized this model in several points but subsequently the model was widely used [6]. Since then, thanks to the memory effect and nonlinear behavior, the memristor found use in various domains, such as neural networks [7–11], programmable analog circuits [12–15], logic gates [16], adaptive filters [17], chaotic circuits [18, 19], and non-volatile memories [20–22].

II. MATHEMATICAL MODELS

Chua, Pershin, and Di Ventra established the electrical relations for memristor, mecapacitor, meminductor as can be seen in [23] and in Figure 1 of [24], where the charge (q), the time-integral of the voltage (ϕ), the time-integral of the charge (σ), and the time-integral of the flux (ρ) are visualized.

A. Memristor Models

Two pairs of equations define the memristor: electrical load control and the magnetic flux control [1, 25].

For electrical load control:

$$v(t) = M\big(q(t)\big)i(t) \quad (1)$$
$$M(q) = d\varphi(q)/dq$$

For magnetic flux control:

$$\mathrm{i(t)} = \mathrm{W}\big(\varphi(\mathrm{t})\big)\mathrm{v(t)} \quad (2)$$
$$W(\varphi) = dq(\varphi)/d\varphi$$

According to the mathematical relations, the electrical resistance of the memristor is not constant but depends on the current that was previously circulated through the device. In 1976, L. Chua introduced dynamic equations to define a memristive system with the property of "pinched hysteresis loop" between current and voltage [25, 26]. According to Biolek, this footprint of the memristif is "self-crossing" which corresponds to a cross with coordinates (0:0) [27]. The pinched hysteris loop/self-crossing was extended to memcapacitor and meminductor.

The HP model's is based on the "modulation" of the size of the doping zone w of the memristor between the value R_{on} and R_{off} as a function of the electrical loads (current) that runs through the component.

$$M(q) = R_{off}\left(1 - \frac{\mu_v R_{on}}{D^2}q(t)\right) \quad (3)$$
$$w(t) = \mu_v \frac{R_{on}}{\mathrm{D}} q(t)$$

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where $M(q)$ is the instantaneous value of the memristor, w the size of the doped zone, D the total size of the doped zone, and μ_v the mobility of the electric charge [5, 6].

B. Memcapacitor Models

The memcapacitance is defined with the electrical relation between the time-integral of the charge (σ) and the time-integral of the voltage (ϕ). It can be either voltage-controlled or charge-controlled depending on its constitutive input variable [25, 28]. In the case of voltage controle, The memcapacitance Cm is:

$$D_m(\sigma) = \frac{d\varphi(\sigma)}{d\sigma} \text{ with } D_m = \frac{1}{C_m} \quad (4)$$

$$\frac{d\varphi}{dt} = v(t) \text{ then, } v(t) = \frac{d\varphi}{d\sigma} \cdot \frac{d\sigma}{dt} = D_m(\sigma) \cdot q(t)$$

C. Meminductor Models

The meminductor represents the link between charge $q(t)$ and the time integral of the flux $\rho(t)$. The mathematical representations of meminductors have two forms: current-controlled meminductor or flux-controlled meminductor [22, 25]. Thus, the meminductance Lm is:

$$L_m(\mathrm{q}) = \frac{d\rho(q)}{dq}, = \frac{d\varphi}{dt}, \Rightarrow L_m(\mathrm{q}).\mathrm{di} = d\varphi \quad (5)$$

Note that, the pinched hysteris loop/self-crossing which corresponds to a cross with coordinates (0 : 0) is footprint of the mem-elements [26, 27].

(a)

(b)

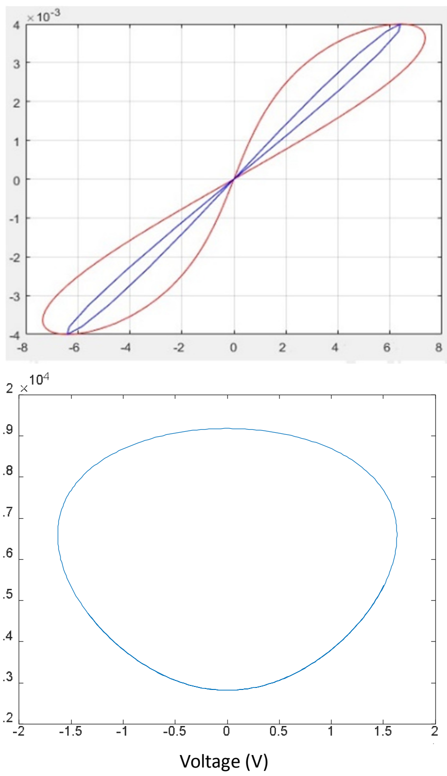


Fig. 1. (a) Pinched hysteresis loop appearing between current and voltage for sinusoidal input with frequency f=10Hz (green), 50Hz (red), (b) Variations of memristif values versus voltage.

III. MATLAB IMPLEMENTATION AND NUMERICAL RESULTS

A. Memristor Implementation

The model was implemented on Matlab. Figure 1 shows the pinched hysteresis loop between current and voltage and the variation of memristor versus voltage. For this simulation, the electrical load control was chosen. Note that if the frequency increases beyond 100Hz, the characteristic becomes a linear line corresponding to Ohm's law.

B. Memcapacitor Implementation

The model was implemented in Matlab and the footprint (pinched hysteresis loop) of the memcapacitor appears under sinusoidal input between voltage and electrical load. Figure 2 shows the results.

(a)

(b)

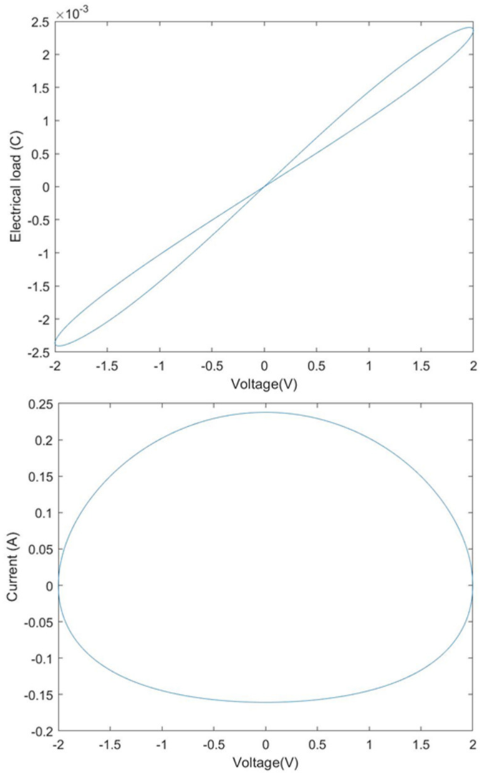


Fig. 2. (a) Voltage and electric load pinch hysteresis loop, (b) variation of current versus voltage.

C. Meminductor Implementation

The model was implemented in Matlab and the footprint (pinched hysteresis loop) of meminductor appears under sinusoidal input between flux and current. Figure 3 shows the numerical results.

IV. EXPERIMENTAL CIRCUIT EMULATORS

To the best of our knowledge, there are no physical implementations of memcapacitor or meminductor circuits. Due to this, there has been an emerging research devoted to the development of emulator circuits of these devices during the recent years. In the literature, different approaches have been proposed for the emulation of memcapacitors and meminductors. Most of them are based on memristor component or its circuit emulator [24, 29-32]. In our case, we chose to develop memcapacitor and meminductor circuit emulators that do not require the use of a memristor or its emulator. In fact, our emulators are based on the same design and are able to emulate either a memcapacitor or a meminductor with minimal changes.

(a)

(b)

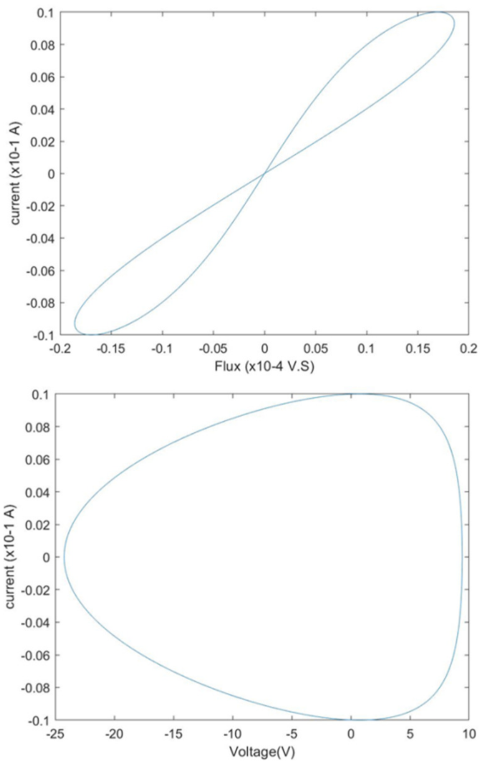


Fig. 3. (a) Flux and current pinch hysteresis loop, (b) variation of current versus voltage.

The circuit emulators are based on voltage/current converter with operational amplifier. The operating principle of the circuits is based on a second output feedback which is connected to the non-inverting input of the amplifier through the capacitor C2. Thus, in both cases, the C2 capacitor provides the memory effect. Figures 4-5 show the circuit emulators and transient simulation results from Ltspice. The pinched hysteresis appears between the voltage source and the current in C2.

The circuit parameters are:

- For the memcapacitor emulator *C1*=*C2*=50nf, *Vf*=(1V,100Hz), *Vin*=(1V,200Hz).
- For the meminductor emulator *L*=10mH, *C2*=50nf, *Vf*=(1V,100Hz), *Vin*=(1V,200Hz).

Frequency simulations of the emulator circuits show that they act as filters. The memcapacitor emulator has a high-pass filter behavior and the meminductor emulator acts as a low-pass filter. In the Figure 6, the frequency simulation (Bode diagram) results can be seen.

(a)

(b)

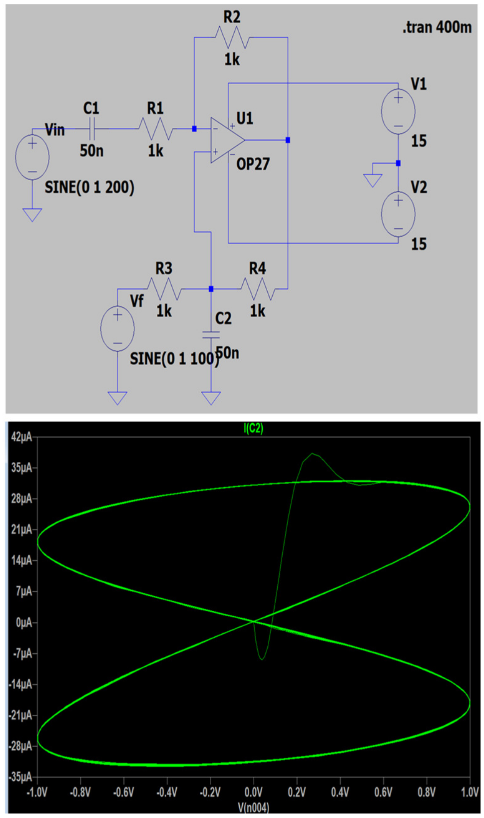


Fig. 4. Memcapacitor emulator.

(a)

(b)

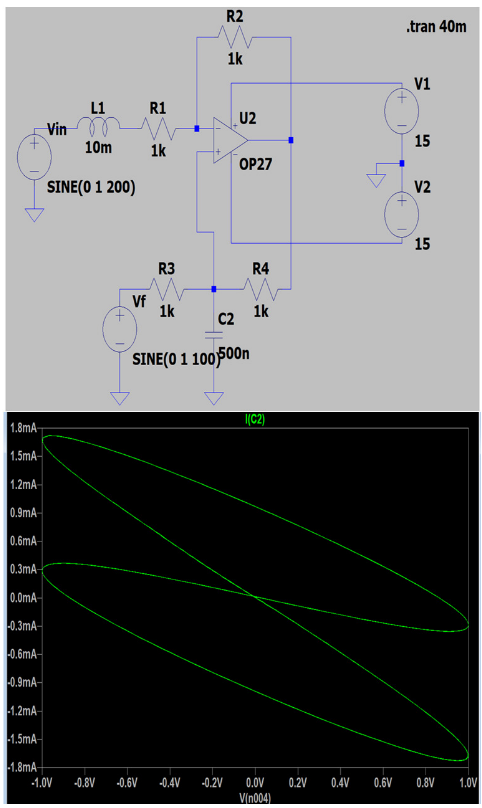
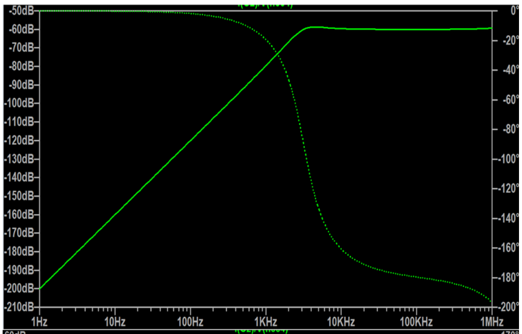


Fig. 5. Meminductor emulator.

(a)



(b)

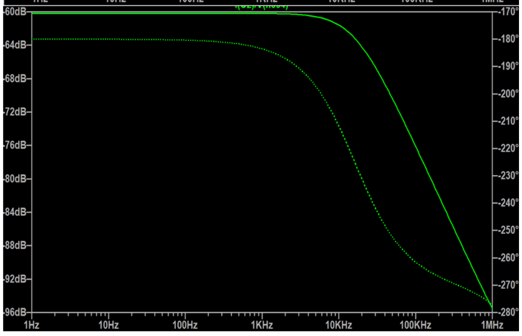


Fig. 6. Frequency simulations of emulators: (a) memcapacitor, (b) meminductor.

In fact, we can show that the circuit emulators have equivalent circuit filters. These circuits can easily be built from passive elements. Figure 7 presents the equivalent circuit filters and Bode diagram results.

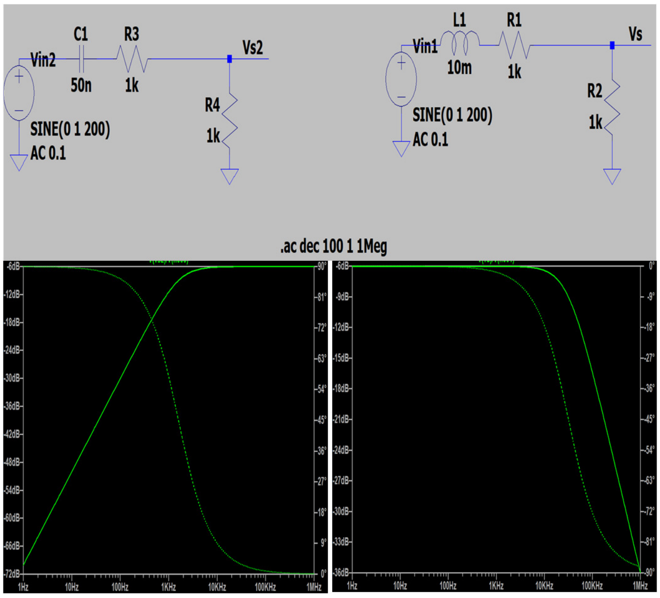
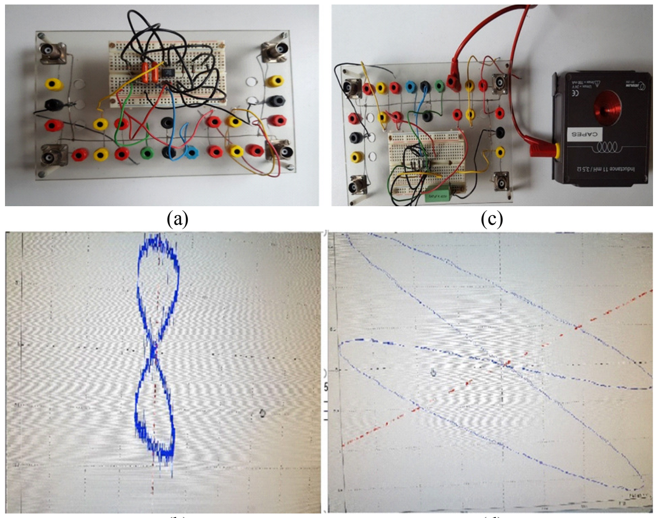


Fig. 7. Equivalent circuit filters and simulation results.

In order to validate the memcapacitor and meminductor emulators, circuit implementations were made. Figures 8-9 show the implementation and the experimental responses of the circuits.



(a) (c)

(b) (d)

Fig. 8. Experimental implementation and results: (a) (b) Memcapacitor, (c) (d) Meminductor.

The obtained results show a good fit between the simulations and the experimental tests. However, during the tests, the memcapacitor and meminductor effects were obtained at lower frequencies than those of the Ltspice simulations. We assume that the implementation of emulators on PCB will achieve better results in terms of operating frequency. Indeed, some parasitic effects will be reduced.

V. CONCLUSION

In this paper, the concepts of memory-elements memristor, memcapacitor, and meminductor were presented. After the presentation of the mathematical models describing the behavior of these components, the circuit emulators for memcapacitor and meminductor, based-on operational amplifier voltage/current converter, were shown. The results show a good fit between the experimental tests and theory simulations.

REFERENCES

[1] L. Chua, "Memristor-The missing circuit element," *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971, https://doi.org/10.1109/TCT.1971.1083337.

[2] K. C. Selvam and S. Latha, "A Novel Voltage Divider Circuit," *Engineering, Technology & Applied Science Research*, vol. 2, no. 5, pp. 278–280, Oct. 2012, https://doi.org/10.48084/etasr.239.

[3] S. N. Asl, M. Tarkhan, and M. S. Nia, "A Gain Programmable Analog Divider Circuit Based on a Data Converter," *Engineering, Technology & Applied Science Research*, vol. 7, no. 6, pp. 2251–2255, Dec. 2017, https://doi.org/10.48084/etasr.1436.

[4] B. L. Dokic, "A Review on Energy Efficient CMOS Digital Logic," *Engineering, Technology & Applied Science Research*, vol. 3, no. 6, pp. 552–561, Dec. 2013, https://doi.org/10.48084/etasr.389.

[5] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008, https://doi.org/10.1038/nature06932.

[6] Y. Kebbati, "Programmable Resistors : Model and Applications," *International Journal of Engineering and Applied Sciences*, vol. 5, no. 3, Mar. 2018, Art. no. 257266.

[7] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale Memristor Device as Synapse in Neuromorphic Systems,"

Nano Letters, vol. 10, no. 4, pp. 1297–1301, Apr. 2010, https://doi.org/10.1021/nl904092h.

[8] Y. V. Pershin and M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Networks*, vol. 23, no. 7, pp. 881–886, Sep. 2010, https://doi.org/10.1016/j.neunet.2010.05.001.

[9] M. R. Azghadi, B. Linares-Barranco, D. Abbott, and P. H. W. Leong, "A Hybrid CMOS-Memristor Neuromorphic Synapse," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 2, pp. 434–445, Apr. 2017, https://doi.org/10.1109/TBCAS.2016.2618351.

[10] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, and D. B. Strukov, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," *Nature*, vol. 521, no. 7550, pp. 61–64, May 2015, https://doi.org/10.1038/nature14441.

[11] R. Kozma, R. E. Pino, and G. E. Pazienza, *Advances in Neuromorphic Memristor Science and Applications*. New York, NY, USA: Springer, 2012.

[12] S. Shin, K. Kim, and S.-M. Kang, "Memristor Applications for Programmable Analog ICs," *IEEE Transactions on Nanotechnology*, vol. 10, no. 2, pp. 266–274, Mar. 2011, https://doi.org/10.1109/TNANO.2009.2038610.

[13] F. Merrikh-Bayat and S. B. Shouraki, "Memristor-based circuits for performing basic arithmetic operations," *Procedia Computer Science*, vol. 3, pp. 128–132, Jan. 2011, https://doi.org/10.1016/j.procs.2010.12.022.

[14] Y. V. Pershin and M. Di Ventra, "Practical Approach to Programmable Analog Circuits With Memristors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 1857–1864, Dec. 2010, https://doi.org/10.1109/TCSI.2009.2038539.

[15] Y. V. Pershin, E. Sazonov, and M. Ventra, "Analogue-to-digital and digital-to-analogue conversion with memristive devices," *Electronics Letters*, vol. 2, no. 48, pp. 73–74, 2012, https://doi.org/10.1049/el.2011.3561.

[16] I. Vourkas and G. Ch. Sirakoulis, "Emerging Memristor-Based Logic Circuit Design Approaches: A Review," *IEEE Circuits and Systems Magazine*, vol. 16, no. 3, pp. 15–30, 2016, https://doi.org/10.1109/MCAS.2016.2583673.

[17] T. Driscoll *et al.*, "Memristive adaptive filters," *Applied Physics Letters*, vol. 97, no. 9, Aug. 2010, Art. no. 093502, https://doi.org/10.1063/1.3485060.

[18] A. Buscarino, L. Fortuna, M. Frasca, and L. Valentina Gambuzza, "A chaotic circuit based on Hewlett-Packard memristor," *Chaos: An Interdisciplinary Journal of Nonlinear Science*, vol. 22, no. 2, Jun. 2012, Art. no. 023136, https://doi.org/10.1063/1.4729135.

[19] B. Muthuswamy and P. P. Kokate, "Memristor-Based Chaotic Circuits," *IETE Technical Review*, vol. 26, no. 6, pp. 417–429, Nov. 2009, https://doi.org/10.4103/0256-4602.57827.

[20] C. Xu, X. Dong, N. P. Jouppi, and Y. Xie, "Design implications of memristor-based RRAM cross-point structures," in *Design, Automation & Test in Europe*, Grenoble, France, Mar. 2011, pp. 1–6, https://doi.org/10.1109/DATE.2011.5763125.

[21] J. Secco, F. Corinto, and A. Sebastian, "Flux–Charge Memristor Model for Phase Change Memory," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 1, pp. 111–114, Jan. 2018, https://doi.org/10.1109/TCSII.2017.2701282.

[22] H. A. F. Almurib, T. N. Kumar, and F. Lombardi, "Design and evaluation of a memristor-based look-up table for non-volatile field programmable gate arrays," *IET Circuits, Devices & Systems*, vol. 10, no. 4, pp. 292–300, 2016, https://doi.org/10.1049/iet-cds.2015.0217.

[23] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proceedings of the IEEE*, vol. 64, no. 2, pp. 209–223, Oct. 1976, https://doi.org/10.1109/PROC.1976.10092.

[24] F. J. Romero, A. Ohata, A. Toral-Lopez, A. Godoy, D. P. Morales, and N. Rodriguez, "Memcapacitor and Meminductor Circuit Emulators: A Review," *Electronics*, vol. 10, no. 11, Jan. 2021, Art. no. 1225, https://doi.org/10.3390/electronics10111225.

[25] A. G. Radwan and M. E. Fouda, *On the Mathematical Modeling of Memristor, Memcapacitor, and Meminductor*. New York, NY, USA: Springer, 2015.

[26] L. Chua, "Resistance switching memories are memristors," *Applied Physics A*, vol. 102, no. 4, pp. 765–783, Mar. 2011, https://doi.org/10.1007/s00339-011-6264-9.

[27] D. Biolek, Z. Biolek, and V. Biolkova, "Pinched hysteretic loops of ideal memristors, memcapacitors and meminductors must be 'self-crossing,'" *Electronics Letters*, vol. 47, no. 25, pp. 1385–1387, Dec. 2011, https://doi.org/10.1049/el.2011.2913.

[28] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "Circuit Elements With Memory: Memristors, Memcapacitors, and Meminductors," *Proceedings of the IEEE*, vol. 97, no. 10, pp. 1717–1724, Jul. 2009, https://doi.org/10.1109/JPROC.2009.2021077.

[29] Y. Babacan, "An Operational Transconductance Amplifier-based Memcapacitor and Meminductor," *Electrica*, vol. 18, no. 1, pp. 36–38, Feb. 2018.

[30] M. Konal and F. Kacar, "Electronically tunable meminductor based on OTA," *AEU - International Journal of Electronics and Communications*, vol. 126, Nov. 2020, Art. no. 153391, https://doi.org/10.1016/j.aeue.2020.153391.

[31] J. Vista and A. Ranjan, "High Frequency Meminductor Emulator Employing VDTA and its Application," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 39, no. 10, pp. 2020–2028, Jul. 2020, https://doi.org/10.1109/TCAD.2019.2950376.

[32] M. D. Ventra and Y. V. Pershin, "On the physical properties of memristive, memcapacitive and meminductive systems," *Nanotechnology*, vol. 24, no. 25, Feb. 2013, Art. no. 255201, https://doi.org/10.1088/0957-4484/24/25/255201.