Design and Implementation of a Second Order Continuous-Time ΣΔ Modulator for ECG Signal Acquisition

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ABSTRACT

The recent developments in biosignal acquisition devices for continuous supervision of cardiovascular signs of high-risk patients require a high-precision and low-power Analog Front End (AFE) circuit. The proposed design adopts Continuous-Time (CT) Sigma-Delta Modulator (ΣΔM) architecture to achieve high resolution and SIgnal-to-Noise And Distortion ratio (SINAD) requirements. The proposed modulator is a second-order CT-ΣΔM with Cascade of Integrators Feed-Forward (CIFF) architecture that consists of a CT loop filter, a single-bit quantizer, and a Digital-to-Analog Converter (DAC). The use of single-bit quantization in the design reduces circuit complexity and power consumption. To use the designed ΣΔM for measuring ECG signals, a bandwidth (B_w) of 150 Hz is considered with a sampling frequency (f_s) of 153.6kHz to achieve an oversampling ratio of 512. The design is simulated in a standard Cadence Virtuoso EDA tool at 180nm CMOS technology, operating at 1.8V supply voltage at the block level. The simulation results for the designed modulator show that SINAD is 104.5dB, the Effective Number Of Bits (ENOB) is 17.06bits, with power consumption of 24μW, and achieves Schreier's Figure-Of-Merit (FOM) equal to 172.45dB.

Keywords-sigma delta modulator; continuous-time; quantizer; DAC

I. INTRODUCTION

Innovations in communications and advances in CMOS technology along with low power design techniques have given impetus to the research in devices intended for the acquisition of biopotential signals. These signals are very weak, having amplitude and bandwidth ranging from μV to mV and from DC to a few kHz [1]. Typical biopotential acquisition systems for acquiring signals such as Electroencephalogram (EEG), Electromyogram (EMG), Electro-cardiogram (ECG), Electrooculogram (EOG), as shown in Figure 1, consist of an Instrumentation Amplifier (IA) to provide adequate gain with low noise, a Low-Pass Filter (LPF) to confine noise bandwidth and an Analog-to-Digital Converter (ADC) that interfaces the AFE and the digital processing unit. Several architectures to design the IA for the AFE of a biopotential signal acquisition have been reported using techniques such as three operational amplifiers [2], differential difference amplifier [3], capacitively-coupled chopper [4], and current-balancing IA [5]. All these techniques have their own advantages and limitations. The LPF circuit designed using OTA-C continuous-time filtering [6] operates in the sub-threshold region to save power for portable ECG signal detection and a second order LPF [7] is used with low noise and low power for programmable AFEs. ADCs also play a significant role in biosignal acquisition and health monitoring integrated circuits [8].

ADCs that are most commonly used for the ECG signal acquisition are Successive Approximation Register (SAR) and oversampled ADCs. SAR ADCs have moderate accuracy and excellent power to performance ratio, but low resolution of 8 to 12 bits [9, 10]. Higher resolution SAR ADCs need high

resolution feedback DACs, resulting in increased area and power consumption. ΣΔ ADCs are oversampled converters, comprising of either a Switched-Capacitor (SC) or a Continuous-Time (CT) ΣΔ Modulator. A state-of-the-art SC implementation provides high precision and accuracy but due to switched integrators it suffers from stringent settling and slew requirements that lead to more power consumption [11, 12]. Compared to SC, CT architecture consumes less power due to inherent anti-alias filtering that obviates the need for a dedicated analog filter required in the signal acquisition system. In order to attain high resolution, wide dynamic range and low power consumption CTΣΔMs are used with active integrators [13-15]. Active RC and Gm-C based are the two types of CTΣΔM structures. This paper discusses the implementation of CTΣΔM with active RC integrators, summer, quantizer, and resistive DAC. The designed modulator exhibits SINAD of 104.5dB and ENOB of 17.06bits. The experimental results are aligned with mathematical model and simulations.

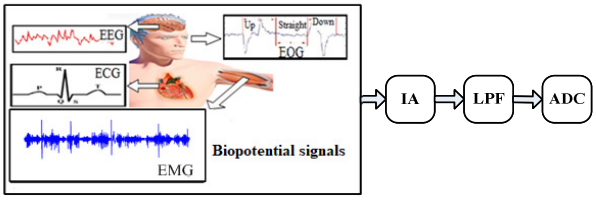

Fig. 1. Block diagram of a biopotential acquisition system.

II. DESIGN METHODOLOGY

The proposed work uses the top-down hierarchical design of ΣΔM synthesis methodology shown in Figure 2.

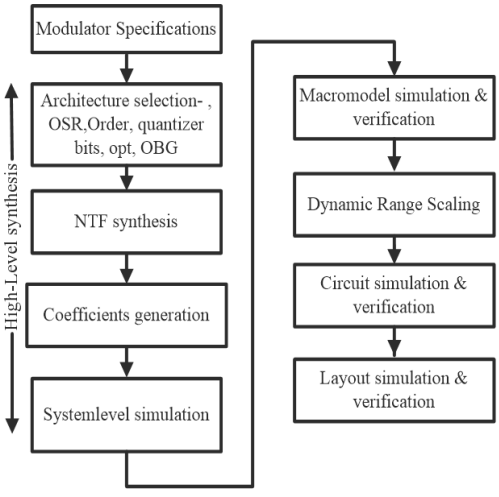

Fig. 2. Design methodology flow graph.

A. Modulator Specifications

For acquiring the ECG signal, the system-level specifications of ΣΔM are set to achieve ENOB of 16-18 bits, SNR > 100dB with sampling rate f_s of around 150kHz and signal bandwidth B_w of 150Hz.

B. Architecture Selection

The design starts with the selection of the Noise Transfer Function (NTF) and the modulator architecture with parameters such as the Oversampling Ratio (OSR) and the order of the modulator (L) and N-bit quantizer. The value of OSR or clock rate is constrained by technology node and power consumption, which varies between 8 and 512 [16]. Higher order modulators having L > 2 improve the SNR significantly, but with an increase in circuit complexity and deterioration of stability. Hence, the proposed design aims for a lower order modulator with higher OSR. The single-bit quantizer is intrinsically linear without mismatch in the quantization step, whereas the multibit quantizer exhibits mismatched quantization steps but has low in-band quantization noise and allows a more aggressive NTF with higher Out-of-Band Gain (OBG), reduced sensitivity to the clock jitter, and lower slew rate requirements from the loop filter [17]. According to the rule-of-thumb [18], for a single-bit quantizer to ensure stability the value of OBG must be about 1.5 and for a multibit quantizer between 1.5 to 3.5. Higher values of OBG cause overloading of the quantizer resulting in modulator instability.

C. NTF Synthesis

ΣΔM employs a NTF implemented using the high-pass Butterworth or inverse Chebyshev transfer function, having a cut-off frequency located outside the signal band. Considering the parameters OSR, L, N, OBG, optimization value and type of filter, the NTF is determined using Schreier's MATLAB Delta-Sigma toolbox [19]. For an ideal L^{th} order system, the NTF is given by $(1 - Z^{-1})^{L}$ with all poles located at Z = 0 and zeros at Z = 1. Spreading these zeros within the signal band and moving the poles within the unit circle, significantly improves SQNR and stability. The modulator becomes unstable if system poles move out of the unit circle.

D. Coefficient Generation

NTF is realized to obtain CTΣΔM coefficients for feedback (FB) and feedforward (FF) form topologies. Each of them is further distinguished by two different forms to generate four topologies - Cascade of Resonators FB (CRFB), Cascade of Integrators FB (CIFB), Cascade of Resonators FF (CRFF), and Cascade of Integrators FF (CIFF).The FB structure consists of several DACs that fed back to all the integrator output and does not require a large summer before the quantizer. In FF structure, a single DAC is required in the FB path without excess loop delay compensation, which is more area efficient [20]. The other advantage of the FF structure is the reduced output swing of the first integrator. Given a certain output range, the first integrator allows a bigger loop gain and hence lower performance requirements on the following stages. However, the FF architecture requires a multi-input adder to sum all the FF branches before the quantizer. In the current work, a CTΣΔM with CIFF architecture is implemented with its state-space representation as shown in Figure 3. The CTABCD matrix is given by (1) along with its description in Table I.

$$[ABCDc] = \left[\begin{array}{cc|c} \multicolumn{2}{c}{\mathbf{A}} & \mathbf{B} \\ 0 & 0 & 1 \\ 1 & 0 & 0 \\ \hline \multicolumn{2}{c|}{\mathbf{C}} & \mathbf{D} \\ 0.6667 & 0.2288 & 0 \end{array}\right] \quad \begin{array}{c} \\ -1 \\ 0 \\ \\ 0 \end{array} \quad (1)$$

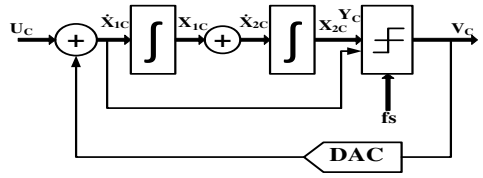

Fig. 3. State-space representation of the CTΣΔM.

TABLE I. DESCRIPTION OF THE ABCDc MATRIX

Matrix & order	Function	Representation
A L×L	Loop filter interconnects	0:No FB connection from X_{1c} to $\dot{X}_{1C}$ 0: No FB connection from X_{2c} to $\dot{X}_{1C}$ 1: X_{1c} directly feeds $\dot{X}_{2C}$ 0: No FB connection from X_{2c} to $\dot{X}_{2C}$
B L×L	Modulator i/p & the f/b DAC o/p to the loop filter.	1: FB connection from U_c to $\dot{X}_{1C}$ -1: FB connection from V_c to $\dot{X}_{1C}$ 0: No connection from U_c to $\dot{X}_{2C}$ 0: No FB connection from V_c to $\dot{X}_{2C}$
C 1×L	K coefficients, i/p from loop filter to the summer.	K_1: Coefficient value from X_{1c} to Y_C K_2: Coefficient value from X_{2c} to Y_C $K_1 = 0.6667$ $K_2 = 0.2288$
D 1×L	Excess loop delay	0: No connection from U_c to Y_C 0: No connection from V_c to Y_C

Based on (1), the obtained block diagram of the 2nd order CTΣΔM with CIFF is as illustrated in Figure 4.

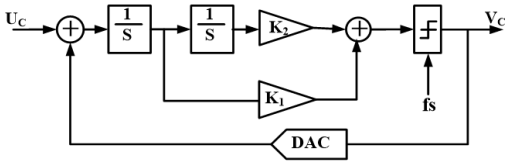

Fig. 4. Block diagram of the second order CTΣΔM with CIFF.

E. System Level Simulation

The behavioral simulation is performed using MATLAB excluding circuit noise to determine the key parameters and individual block specifications. To use the designed ΣΔM for measuring ECG signals, bandwidth of 150Hz is considered with a sampling frequency of 153kHz. For OSR=512, L=2, N=1, OBG=1.5, opt =1, the pole-zero plot by which design stability is verified and the frequency response of NTF is illustrated in Figure 5. The pole-zero map of the 2nd order system has two complex conjugate poles (marked with X) and two zeros (marked with O) at dc that suppress the in-band quantization noise. Frequency response shows that the OBG is 3.438dB (1.5). The resulting NTF is given by:

$$\text{NTF}(z) = \frac{Z^2 - 2Z + 1}{Z^2 - 1.225Z + 0.4415} \quad (2)$$

The time domain response of ΣΔM with a two-level quantizer is shown in Figure 6. For a sinusoidal input, the output is pulse-density modulated. The density of the pulse output waveform varies with input amplitude. The frequency domain response of the designed CTΣΔM is shown in Figure 7 in which the power is maximum at the input frequency of the signal and it clearly exhibits 2nd order noise-shaping with a slope of 40dB/decade. The ΣΔM achieves high resolution by the combination of oversampling and noise shaping. For the designed modulator, the MATLAB simulation depicts in-band SNR of 103.85dB at input amplitude of 0.5V with ENOB of 16.96 bits as shown in Figure 7.

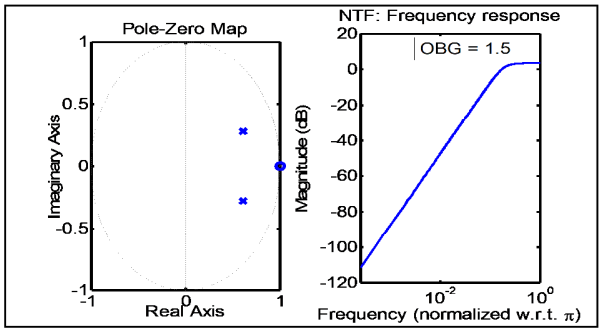

Fig. 5. Left: pole-zero plot, right: NTF frequency response.

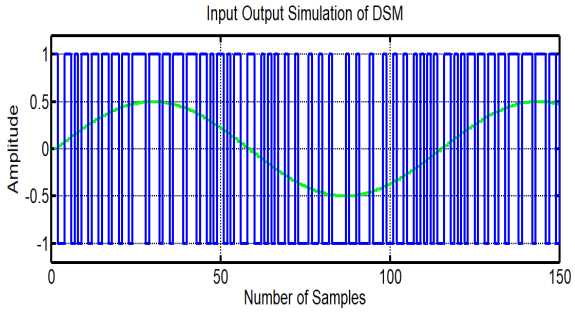

Fig. 6. Time domain plot of input and output with 2-level quantizer.

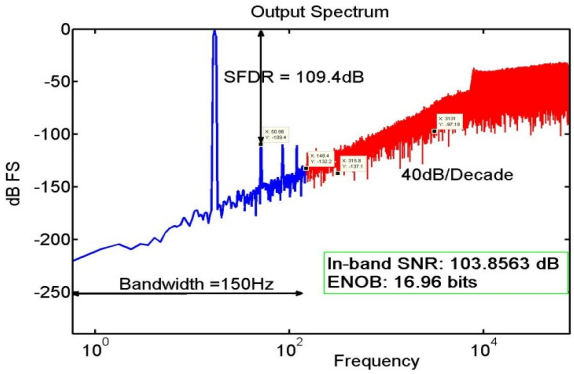

Fig. 7. Measured output spectrum.

The obtained value of peak SNR of 122.7dB at -1.7dBFS input signal with dynamic range of 120dB is shown in Figure 8. The values of in-band SNR and ENOB for different values of OSR of 2nd order CTΣΔM is shown in Figure 9. It's observed that SNR increases with OSR at the rate of approximately 13dB/octave.

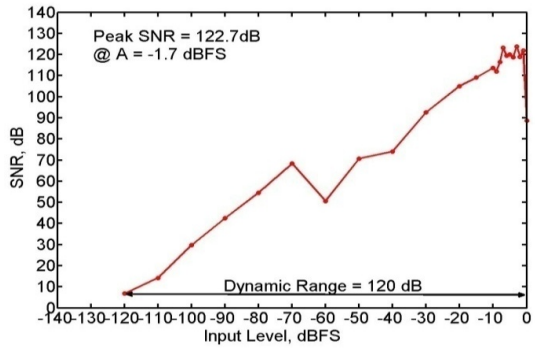

Fig. 8. Measured SNR versus input level.

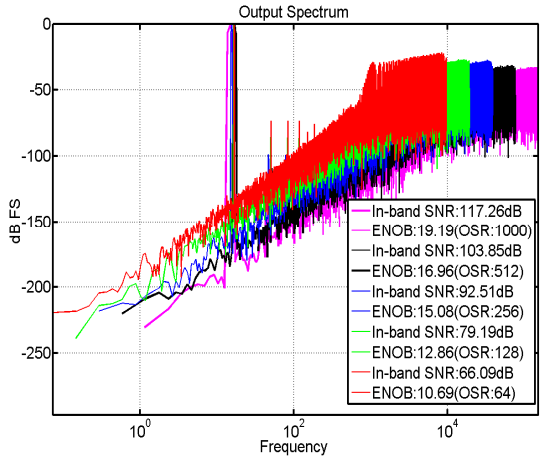

Fig. 9. PSD of the modulator output with values of SNR and ENOB for different OSR values.

F. Macro Model Simulation and Verification

The obtained system-level behavioral model of the ΣΔM architecture that satisfies the required specifications was translated into a macro model consisting of active and passive components in standard CMOS technology using cadence spectre. Ideal building blocks (clock generator, integrators, quantizer, and DAC) [21] were used for validating the design architecture. The schematic of the single-ended 2nd order CT active RC type ΣΔM is shown in Figure 10.

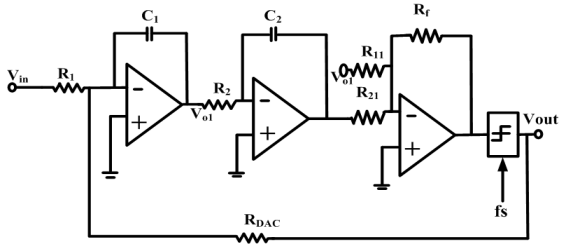

Fig. 10. Schematic of single ended 2nd order CTΣΔM.

The schematic is composed of a single-loop, CIFF structure, and single-bit feedback DAC. Active integrators are used to obtain the low power 2nd order CT system, VerilogA model for a single-bit quantizer, and resistive DAC. Ideal switch and RESET signal are used across the integrator capacitors at the beginning of the simulation. When the RESET is high, the switch is shorted and sets the DC voltage on the integrator output.

The values of the active RC integrators are calculated by using the sampling frequency f_s. The summer circuit is designed using the K-coefficients. The designed values are $R_1 = R_2 = 100K\Omega$, $C_1 = C_2 = 66.67pF$, $R_f = 100k\Omega$, $R_{11} = 150k\Omega$, $R_{21} = 437.06k\Omega$. The simulation of the designed modulator with macro models is carried out using the components from analogLib and ahdlLib of cadence for a signal with input amplitude of 0.25V, 150Hz bandwidth, and 153.6kHz sampling frequency. The swing of integrators, summer, quantizer, DAC before scaling is shown in Table II. Before scaling, the integrator outputs were saturated having values more than the supply voltage, hence through scaling the output voltage levels were reduced.

G. Dynamic Range Scaling

An integrator's output doesn't respond to changes in its input if it saturates. In order to avoid integrator saturation, the loop filter coefficients were scaled without modifying the loop filter transfer function. This is referred to as dynamic range scaling. The values of active RC integrators are calculated using (3) where f_s is the sampling frequency and α and β are scaling coefficients.

$$f_s = \frac{1}{\alpha R_1 C_1} \quad \text{and} \quad f_s = \frac{1}{\beta R_2 C_2} \tag{3}$$

The weighted addition of the integrator outputs is carried out using a summing amplifier. The design of the summing amplifier is calculated using the K-coefficients obtained from Table I.

$$K_1' = \frac{K_1}{\alpha} \; ; \qquad R_{11} = \frac{R_f}{K_1'} \tag{4}$$

$$K_2' = \frac{K_2}{\alpha\beta} \; ; \qquad R_{21} = \frac{R_f}{K_2'} \tag{5}$$

The lower and upper limits for R and C are set by the matching consideration and thermal noise level that is fixed by the overall dynamic range requirements. Table II shows the value of the output swing across different blocks before and after scaling. It is clear that after scaling the voltage levels are reduced, maintaining the desired SNR. The obtained parameter values before and after scaling are shown in Table II.

TABLE II. OUTPUT VALUES BEFORE AND AFTER SCALING.

Parameters	Before scaling	After scaling
Integrator-1	-0.375 to 2.19V	0.46 to 1.34V
Integrator-2	-0.94 to 2.69V	0.32 to 1.42V
Summer	0.023 to 1.69V	0.20 to 1.56V
Quantizer	0 to 1V	0 to 1V
DAC	0 to 1.8V	0 to 1.8V
Signal power input	-12.04	-12.04
Signal power output	-17.15	-17.15
Sinad input	234.8	234.8
Sinad output	-13.97	-13.97
SINAD	102.02	104.5
ENOB	16.65	17.06

III. SECOND-ORDER CTΣΔM

The proposed modulator is a 2nd -order CTΣΔM with CIFF architecture that consists of a CT loop filter, single-bit quantizer, and resistive DAC as shown in Figure 11. Fully differential architecture implementation minimizes even-order harmonics and common-mode noise [22]. The circuits implemented with active RC integrators are highly linear, insensitive to parasitics, and simple to design. The first stage processes in-band and DAC signal. The designed values of the first stage integrator input resistance R_1 and capacitance C_1 are 100kΩ and 161.8pF respectively. In order to reduce power and to enhance the linearity of the modulator, R_1 is maximized up to the input-referred thermal noise, P_N given by:

$$P_N = 8kTB_w\left[R_1 + R_{DAC}\frac{{R_1}^2}{{R_{DAC}}^2} + \frac{2}{3g_{m,OTA}}\left(1+\frac{R_1}{R_{DAC}}\right)^2\right] \quad (6)$$

where k, T, B, R_{DAC}, $g_{m,OTA}$ represent the Boltzmann constant, the absolute temperature, signal bandwidth, feedback DAC resistors, and amplifier input transconductance, respectively. The values of the 2nd stage integrator R_2 and C_2 are 200kΩ, 41.89pF, respectively.

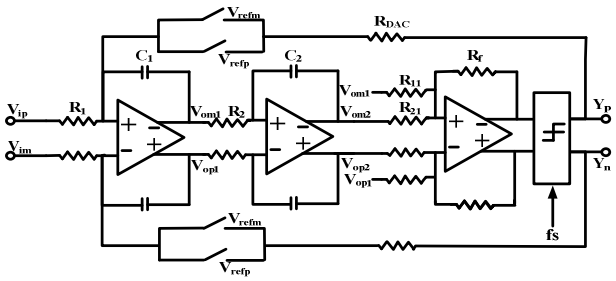

Fig. 11. Schematic of the fully differential 2nd-order CTΣΔM designed with active-RC type.

The summing amplifier uses the resistors R_f = 80kΩ, R_{11} = 61.8kΩ, R_{21} = 143.26kΩ designed using (4) and (5) FF coefficients. Switched-resistor feedback DAC, R_{DAC}, is chosen to be equal to R_1 for better matching performance that provides less noise [23] than the current-steering DAC.

IV. MEASUREMENT RESULTS

The presented modulator has been implemented in 180nm CMOS technology at 1.8V supply voltage, for applied input of a sinusoidal signal of 45Hz with input amplitude of 0.25V and sampling frequency of 153KHz achieving OSR of 512. For Hanning window of 16384-points, the block level simulation depicts SINAD of 104.5dB with ENOB of 17.06 with a power consumption of 24μW and achieves Schreier's Figure-of-Merit of 172.45dB. Table III shows the performance comparison of the proposed work with other known methods, showing an increase in the values of SINAD and ENOB.

V. CONCLUSION

This paper proposes the CTΣΔM design for the acquisition of ECG signals. The cascade of integrators with FF is opted for the implementation of loop filter, with active-RC integrators and resistive feedback DAC that reduces noise and power dissipation. The set target of ENOB is attained by the systematic coefficient generation using MATLAB and the loop filter coefficients scaling using the cadence EDA tool. The designed modulator implemented in 180nm CMOS technology with signal bandwidth of 150Hz, high OSR of 512 has SINAD of 104.5dB and ENOB of 17.06 achieving around 10% increase in comparison with existing techniques. The modulator consumes 24μW power from 1.8V supply and achieves Schreier's FOM of 172.45dB.

TABLE III. CTΣΔM PERFORMANCE COMPARISON

Reference	[15] [b]	[24][a]	[21][a]	Proposed
Year of publication	2021	2018	2012	
Technology [nm]	180	180	180	180
Bandwidth	2KHz	200Hz	20KHz	150Hz
OSR	256	256	512	512
SINAD in dB	94.28	96	87.3	104.5
ENOB *	15.37	16	10	17.06
Power	32.34 μW	-	-	24μW
FoMs **	177.9dB	-	-	172.45dB

**FoMs in dB = SINAD + $10\log_{10}\left(\frac{B_W}{Power}\right)$, *ENOB = $\frac{SINAD-1.76}{6.02}$,
[a] block-level simulation, [b] transistor-level simulation

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