A Novel Architecture Design of a USB Module in Wireless Modem for IOT Applications

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ABSTRACT

Embedded micro-electro-mechanical technologies and network connectivity allow for the integration of sensing, identification, and communication capabilities into a variety of smart devices. These intelligent devices can automatically link to create the Internet of Things (IoT). The greater power consumption of a scan-based test has been one of the biggest problems since Very Large-Scale Integration (VLSI) architecture was introduced. There are too many switches made during the scan shifting procedures due to the enormous number of the scan cells. The design and implementation of an IoT access point are presented in this paper using the Logic Vision tool. In the semiconductor sector, scan chains are frequently employed for structural testing following fabrication or production. In this paper, a new architecture was designed with USB protocol, which reduces dynamic power, and fault-free circuits were constructed. The proposed architecture can work with the current one without changing the decompression architecture. Experimental findings on commercial circuits demonstrate that this strategy minimizes the scan shifting power.

Keywords-scan chains; logic vision; JTAG; USB; Design-for-Testability (DFT); Logic Built-In Self-Test (LBIST)

I. INTRODUCTION

Nowadays, over 100 million logic gates are present in the contemporary chip architectures [1]. In particular, this large chip architecture features a lot of scan cells, which result in too many switching operations during the test mode. More dynamic power consumption and IR-drop are produced by these activities [2]. Unfortunately, the test operation consumes far more power than the functional operation [3], due to the fact that when the scan chains are used to load and unload test patterns, the scan flip-flops go many times through altering states. As a result, the toggling phenomena shift to the internal combinational logics, and these logics' switching activities drastically increase [4]. This issue may reduce the quality of scan tests by causing structural harm to packages, bonding wires, or silicon [5]. Both peak and average test powers should be taken into consideration with a view to mitigating these damages. The average power is defined as the energy consumption needed to test the duration ratio [3], while it increases chip heat dissipation. Increasing temperature and current density demand pricey test kits that can withstand extreme heat [6]. However, the peak power, or the greatest power in a cycle, results in inaccurate data transfer and invalid test findings [7].

Integrated Circuit (IC) testing is essential for the semiconductor industry. It examines whether a circuit operates as intended to assure the product's quality. Moore's law has caused reduction in feature sizes in the VLSI era, which

increases the likelihood of manufacturing flaws leading to faulty circuits. To improve production and lower cost, effective tests must be created to find these defects and determine the root of these silicon problems. Functional testing and structural testing are the two basic types of evaluating digital ICs. Each entry of the truth table will be functionally tested in every respect using the supplied inputs. Although feasible, a real circuit with hundreds of input lines would make the usage of such a test impracticable because it would require too much time [8, 9]. The foundation of structural testing is the employment of vectors with gate-level accuracy that test every flaw in the circuit. These vectors are produced by implementing Automatic Test Pattern Generators (ATPGs), such as Synopsys' TetraMAX [10, 11] or Cadence's Encounter True-Time ATPG [12], deployuing the netlist simulation. Usually, scan chains are inserted into the design to obtain good fault coverage during the structural testing. This is automatically accomplished through transforming the flip-flops into scan flip-flops and attaching them to large shift registers. In addition to the circuit's input/output pins, the scan chain provides the tester with an extra means of loading input patterns (by shifting in vectors in the scan chain) and unloading response vectors (by shifting out). Without a full scan, a circuit can also be structurally tested, though in some cases the fault coverage may suffer. After chip manufacturing, structural testing is often carried out at the fab using pricey testers like Automatic Test Equipment’s (ATEs).

In the semiconductor sector, scan chains are frequently utilized for structural testing following fabrication or production. Internal connections between these scan chains and the IEEE Std 1149.1 JTAG (Joint Test Access Group) [13], Test Access Port (TAP) provide the tester/user with an external interface. JTAG can be applied to debuggers, as well as to devices that require programming or upgrading, including pay-tv subscription set-top boxes. JTAG can also be deployed to upgrade the operating system on some smartphones or to program bitstreams in FPGAs. Even though scan chain DFT offers the best testability, an attacker can exploit it to access internal chip data, retrieve confidential data that have been stored, and figure out where every secret element in a chain is located. Scan chains could be permanently turned off after chip testing (by, for example, blowing some fuses), but then the chip's ability to be tested in the field is gone. On some of these damaged scan chain elements, probing attacks are still possible, and even blown fuses can be carefully reconnected. Incorporating these fuses might also be rather expensive regarding the area.

II. EXISTING DESIGN-FOR-TESTABILITY (DFT) METHODS

Many strategies have been put forth to protect the delicate data in the Circuit Under Test (CUT). Authors in [14] made the suggestion that a side channel attack could be utilized to extract the chip's private data. The complete scan chain is broken into smaller units and every unit is linked together by an arbitrary key circuit in [16]. An unauthorized user can only access randomly produced data when attempting access. Because the data are random, this method is more secure. This technique's main disadvantage is that it uses more sub chains, increasing both power and connection complexity, and thus becoming more bewildering. In order to shorten the scan time needed for testing, authors in [17] suggested a plan that uses a lock and key protected approach which divides the whole scan chain into identical-length sub chains. A LFSR module chooses a collection of scan chains for the test operation while keeping the remaining chains idle. This method's disadvantage results from an extra module that raises the area above. Another method was suggested in [18] to safeguard Intellectual Property (IP). This method engages scan chain partitioning and inserts a private key to access the test vectors. The keys are kept in dummy flip flops that are connected to a key checking module [19]. The random sequence is generated if the key verification is unsuccessful. Otherwise, the scan data are unloaded. A new method, proposed in [15], replaces the traditional scan chain architecture with the de Bruijn graph method, hiding the original data from hackers. A new key-based structure with a series of unique keys contained in the test vector is proposed in [20]. Scan data are activated when the key matches the original key. The JTAG interface side channel attack is covered in [14]. The JTAG is protected by a secure manner in this article, and the system is completely walled off to outside users. To maintain security, authors in [21] proposed a novel method utilizing two stages of key authentication. The scan chain is essentially split into two sections: the first section is utilized for key authentication, while the second section is used for regular scan operations. Turning off the scan chain flip flops prevents a response from being made in the event that the verification of the first component key is unsuccessful and an attack is identified. The size of the input vectors is increased by the usage of a collection of authentication keys. The techniques listed above are mostly focused on high level security with limited testability. However, there is not any widely accepted, low-cost secure solution for preventing random testing. To reduce dynamic power, the steps mentioned below can be considered:

- Reduced power supply voltage V_{dd}
- Reduced voltage swing in all nodes
- Reduced switching probability (transition factor)
- Reduced load capacitance

When the weight of the additional logic is manageable, the DFT-based approach typically surpasses the ATPG-based solution in terms of power consumption reduction. In this study, a new DFT-based method that successfully utilizes scan clock gating, requiring additional hardware is offered. To ensure high controllability, the suggested method has a minimal area overhead and a low level of complexity.

Compaq, Intel, Microsoft, and NEC created the Universal Serial Bus (USB) specification, which was later followed by Hewlett-Packard, Lucent, and Philips. These firms established the USB Implementer Forum to publish the specifications and plan future USB development. An industry-standard addition to the PC architecture, the USB is designed with an emphasis on PC peripherals. The primary objective of the USB protocol was to replace the PC's ever-increasing variety of communication connectors. For instance, a single connection might now take

the place of serial, parallel, and PS/2 ports. The USB will perform the same function and is appropriate for all the applications and peripherals. It is currently the protocol of choice for the majority of PC peripherals due to its complete support for real-time data, voice, audio, and video. The USB is a multipurpose protocol that can support a variety of solutions because it is capable of understanding different PC configurations and form factors. Since the USB is a general standard, products can quickly adopt its interface and increase the PC's functionality by enabling new classes of devices and giving the USB the ability to be used in newly designed devices as technology progresses. USB 3.0 has completed backward compatibility with devices made in accordance with earlier USB specifications. It is similar to the earlier USB 2.0 version and has a dual-bus architecture that allows for retrograde compatibility with USB 2.0. It permits the simultaneous use of Super Speed (5 GBPS) and Non-Super Speed (high speed, 480 Mbps). The USB is a master/slave bus. This indicates that the whole communication on the bus is initiated by the master and the slave can only reply to the master. A PC serves as the master for USB connections, while the device as the slave. Because of this arrangement, USB interruptions are not possible. The host can carry out low-latency device polling to simulate an interrupt thanks to the USB's support for a pseudo-interrupt scheme incorporating low-latency interrupt endpoints. The resilience of the USB protocol is its main benefit. Due to its signal integrity, the USB can utilize shielding, differential drivers, and receivers. Error recovery for data and control fields is performed by the CRC checking mechanism. USB does attachment and detachment detection as well as resource configuration at the system level. USB supports a self-recovery mechanism for corrupted or missing packets utilizing timeouts. USB also supports flow control for streaming data to ensure isochronism and hardware buffer management. Other functions include data structures and control pipes that guarantee independence from unfavorable interactions between functions.

A. Basic Architecture

There are two main ways to eliminate unnecessary test power in research studies and increase the effectiveness of scan-based testing: Automatic Test Pattern Generation (ATPG)-based and DFT-based. One of the strategies for low power management mechanisms that is most frequently used in practice is clock gating. It allows to stop the clock of an extra flip-flop during a present cycle. The connection amid the clock signal ports and the flip-flop typically includes AND gates. To use clock gating, all scan cells are categorized into a number of groups. An illustration of the scan structure with two multiple scan chains and three groups can be seen in [22]. Every group participates in a scan clock (SCK), and each SI is directly connected to each scan cell in a scan chain. Consequently, when their group is triggered by a SCK, the scan cells value is inputted. In the scan test mode, the SE signal either decides the launch and capture mode or the shifting mode is being used for the present test operation. One SCK is triggered by the deMUX selection (SEL) value when the SE is set to "1". On the other side, when the SE is "0", all SCKs are activated, therefore it handles launch and capture. Additionally, an XOR gate is positioned on each scan chain and is connected to all SO ports. There is no issue with loss on the output stage of the test findings because the outputs can be seen through the XOR gate once in every cycle. As it was already indicated, a SI port is connected to each flip-flop in a scan chain. Consequently, it lessens the numerous switching actions brought on by the serial insertion of shifting patterns. Additionally, the shift-out power is eliminated by the way the SO ports are connected. Section IV presents the outperformed power decrease.

B. The Proposed Architecture

The proposed architecture was constructed deploying the JTAG TAP Controller. JTAG is a programming and update tool that can be utilized in debuggers and in devices like pay-tv set-top boxes [23]. Additionally, bitstream programming in FPGAs and operating system upgrades in certain smartphones can be accomplished with JTAG. The Scan bypass control knob was connected to three blocks of internal scan chains to which scan inputs are given and scan outputs are obtained. The Logic Vision (LV) tool of Verdi software was employed in the architecture due to its speedy operation.

There are a few rules of thumb to remember regarding scan bypass clocks:

- Internally generated clock must be bypassed, as displayed in Figure 1. Internally generated clocks are those that come from clock dividers or PLL's in the core.
- Clocks coming from the clock_gen module do not need to be locally bypassed since they are already bypassed in the clock_gen module.
- External clocks are got from pads.

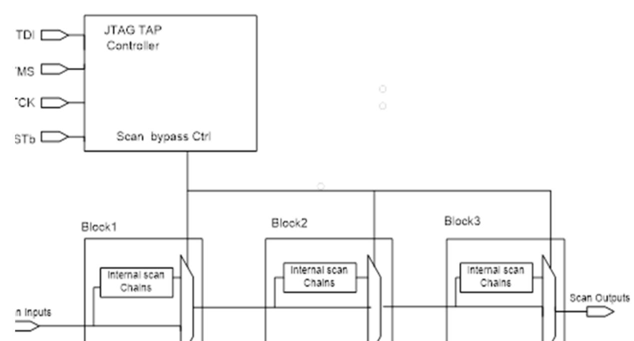

Fig. 1. Bypassing an internally generated clock in scan bypass mode.

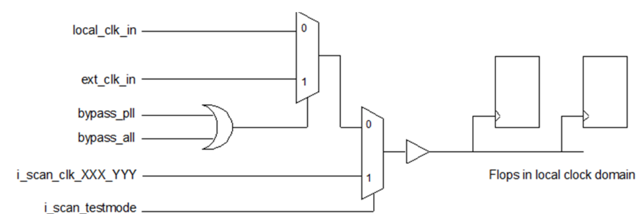

Fig. 2. Scan clock mux structure deployed before the clock broadcast.

The scan bypass clocks are named "i_scan_clk_xxx_yyy", where xxx is an abbreviation for the name of the functional core and yyy gives some indication of what clock is being bypassed. The block uses scan_ctrl, scan_ctrl_clk,

scan_testmode, and hw_reset_ to generate individual scan_block_sel signals for each block in the chip. The chip's scan chain inputs are stitched from block to block and ultimately go to the chip's scan chain outputs. Within each block, the scan chains are either fed through the flip flops in the block, or bypass them and go immediately through the scan mux and out to the next block. There are two clock inputs to this module. The first one is directly from the fast clock from the pad. Note that during the scan operation, the logic which creates this clock input must function normally (i.e. it must not be scanned). The second clock input (slow CLK) is directly from the chip pin. Scan enable is asserted only during the scan shift. The inputs of all the flops are connected to the scan enable. The scan mode is asserted during the entire scan testing process. It is used for various mode/bypass functions.

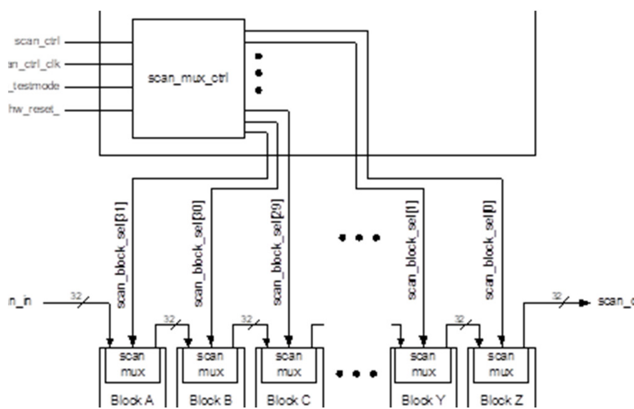

Fig. 3. Connecting scan chains and scan_block_sel signals to the chip's layout blocks.

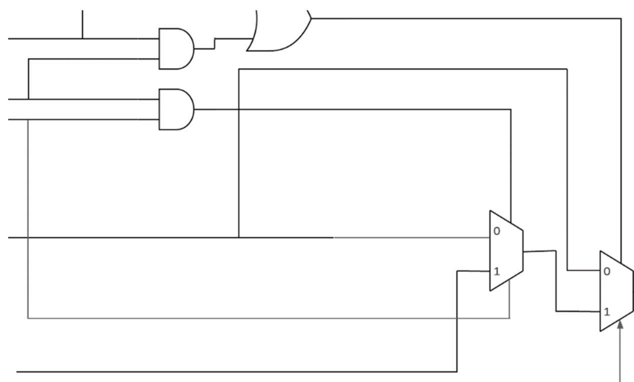

Fig. 4. Block diagram of a clock structure used.

The advantages of having distributed scan architecture are:

- Design handoff of test ready (COMPLETE) cores.
- Faster analysis and verification (shorter runtimes, only needs to be done at one level).
- Improves timing closure predictability.
- Faster ECO turn-around.
- Support for at-speed test for most blocks.
- Simplifies core re-use (within a design or across multiple designs).
- Powerful diagnostic and debug capabilities.
- Allows tight integration into the design flow.

The waveforms of the various signals obtained using the LV interface of the Verdi software are portrayed in Figure 5.

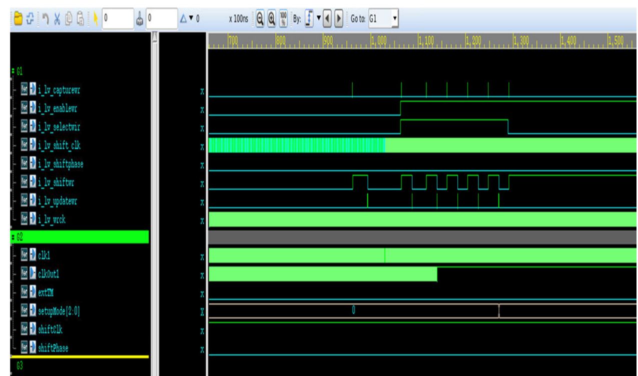

Fig. 5. Waveforms obtained in Verdi using the LV interface.

III. TESTING METHODOLOGY

A. At Block Level

- Need to make sure that each block complies with DFT methodology. All the clock resets are controlled.
- All flops are resettable to make sure which flops do not come under scan.
- This study used the LV tool (lbist) for block level, so it is required to run the basic scan insertion flow on the block and see if there are any changes needed in the block to let the DFT flow run smoothly.
- It is necessary to certify that the memory is in compliance with the foundry standards, and provide a proper wrapper and controller so that the memory related tests can be run as a part of the DFT process.
- Memory repair logic has to be integrated and tested.

B. At Chip Level

- The ATPG patterns were used to test the paths across the blocks to check in the DFT. To accomplish this the TK test compress tool was employed.
- Test methodology at chip level has to be established.
- As per the test methodology, it is advisable to make sure that all the clocks have been controlled and reset in the test mode.

Later, tests for all the above scenarios need to be developed at block and chip level and be verified with timing and not timing simulations. SDF was utilized for timing simulations generated at chip level STA and other sdfs will be generated at different macro levels where applicable. STA was also performed for DFT in all modes at block and chip level to

ascertain that there are sufficient timing margins. For any AISC to obtain maximum yield and to provide good quality product to the customer, the chip has to be thoroughly tested and diagnosed for manufacturing defects and functional errors. The manufacturing defects can be caught and either fixed or provide feedback to the foundry or the design team by the DFT setup in the ASIC. There are many techniques present to generate optimum patterns that cover all the possible faults in the ASIC and also to reduce test time.

IV. RESULTS

Tables I and II show the scan results of the basic and the proposed architecture, respectively. A look at the coverage information reveals that a smaller number of vectors are required in the proposed flow compared to the basic flow, which will give a lot of leverage on the test time. Also, timing closure was achieved in the same clock structure. In this case, the shift power remains the same.

TABLE I. SCAN STATISTICS FOR THE USB BLOCK WITH BASIC SCAN ARCHITECTURE

Design	Total faults		Fault coverage		Vectors	Stuck at test coverage			Transition test coverage			Bridge coverage estimates	
USB	*SA*	*Tran*	*SA*	*Tran*		*N=1*	*N=6*	*N=10*	*N=1*	*N=6*	*N=10*	*SA*	*Tran*
LBIST	5133200	4687913	88.48	82.3	32768	92.06	86.49	84.11	85.74	76.1	72.88	90.62	81.86
Stand alone	5133200	4687913	94.41	90.15	11680	96.44	95.64	93.65	95.93	90.86	85.85	97.1	93.65
Scan burst top off	5133200	4687913	96.66	90.37	13365	96.43	95.6	93.24	95.83	91.43	85.71	97.08	93.67

TABLE II. SCAN STATISTICS FOR THE USB BLOCK WITH PROPOSED SCAN ARCHITECTURE

Design	Total faults		Fault coverage		Vectors	Stuck at test coverage			Transition test coverage			Bridge coverage estimates	
USB	*SA*	*Tran*	*SA*	*Tran*		*N=1*	*N=6*	*N=10*	*N=1*	*N=6*	*N=10*	*SA*	*Tran*
LBIST	5494440	5128196	92.25	87.07	32768	93.99	90.02	88.14	89.27	81.47	78.47	92.97	85.94
Stand alone	5494440	5128196	95.68	93.84	7945	97.49	95.55	93.74	96.22	90.44	86.1	97.13	93.86
Scan burst top off	5494440	5128196	95.68	93.74	14138	97.48	95.72	93.38	96.11	91.68	85.97	97.15	94.01

A. Area Utilization

Table I describes the traditional scan chain that uses the entire area. However, in order to provide security, new modules are added to the current methods, which also take up more space. The suggested approach, which utilizes an extra block with less space above the previous one, provides security [5, 7], as illustrated in Tables III and IV. The area overhead caused by the LFSR and multiplexer is dependent on the number of instances and scan chains.

TABLE III. TOTAL DFT AREA OVERLOAD WITH THE BASIC SCAN ARCHITECTURE

Group	Cell area percentage	Cell area	Number of instances
LTEST Total	5.83	28166.88	8890
MBIST Total	3.46	16483.28	40

TABLE IV. TOTAL DFT AREA OVERLOAD WITH THE PROPOSED SCAN ARCHITECTURE

Group	Cell area percentage	Cell area	Number of instances
LTEST Total	5.72	27811.23	9611
MBIST Total	3.44	16422.34	40

In the basic architecture, for LTEST when the number of instances was 8890, the cell area occupied was 28166.88 and the percentage was 5.83. For MBIST, when the number of instances was 40, the cell area occupied was 16483.28 and the percentage was 3.46. In the proposed architecture, for LTEST, when the number of instances was 9892, the cell area occupied was 28862.46 and the percentage was 6.03. For MBIST when the number of instances was 40, the cell area occupied was 16483.28 and the percentage was 3.45.

B. Power

The circuit designs of modern technology are increasingly complex and contain hundreds or even thousands of scan flip flops. The proposed solution was put into practice utilizing an equilibrium chain structure, which also decreases power usage and makes the actual time proportional to the power. The incorporation of the secured modules reduces the proposed method's power overhead by a small proportion. Figure 6 depicts the summary of the power analysis, which is manifested as dynamic currents for the basic and proposed topologies.

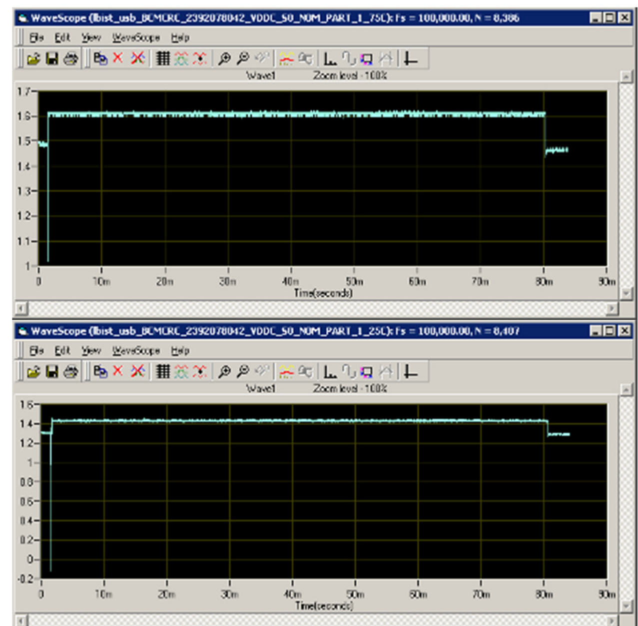

Fig. 6. Dynamic currents for the basic and proposed architectures.

V. CONCLUSION

In this paper, a Logic Vision scan methodology is introduced. The particular method relies on the gating of the clock of several groupings via lowering the internal combinational logic's toggling rate. The suggested method yields excellent results, engaging little energy and space. Applying the proposed approach to a variety of benchmark and commercial circuits yielded experimental findings demonstrating that it performs well in all situations regardless of the size of the circuits. Additionally, this technique is compatible with already-used compression techniques, including broadcast-based test data compression and linear-decompression. In conclusion, the proposed approach might work well for big circuits with a small area overhead.

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