Optimizing Switching Activity using LFSR-Driven Logic for VLSI Circuits

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ABSTRACT

In Very-Large-Scale-Integration (VLSI) designs, thorough testing is indispensable for identifying the structural defects of the chip. Timely detection and correcting serious defects are pivotal in preventing faulty chips from reaching customers and avoiding failures. In scan designs, the toggling activity is a critical factor due to the defects between lower cells and metal layers, exacerbated by diverse Process, Voltage, and Temperature (PVT) conditions. These defects significantly impact design testability, quality, and reliability, necessitating meticulous testing to ensure that chips meet the desired specifications. Effectively managing power consumption in the current VLSI landscape is crucial amid the ongoing energy crisis. Balancing the need for Low-Power (LP) with the complexity of integrating transistors onto a single silicon substrate poses significant challenges. As chip densities increase, power dissipation during testing surges, adversely affecting durability, performance, cost, and reliability. Engineers are racing to optimize test power usage, employing advanced Design for Test (DFT) techniques to incorporate efficient power management into Silicon-on-Chip (SoC) designs. Linear Feedback Shift Registers (LFSRs) are phenomenal in addressing DFT parameters like power, and performance, and for better pseudo-random pattern generation. Hence, this paper proposes a groundbreaking approach to power reduction techniques deploying the LFSR architecture, and thus challenging conventional scan-based testing methods. The proposed LFSR architecture is meticulously designed and rigorously tested using Cadence DFT Modus solution on ISCAS'89 benchmarking circuits. Coverage was unequivocally evaluated for Quality of Results (QoR) metrics, such as fault coverage, memory usage, pattern counts, switching activity, fault testing, and runtime. The specific evaluation clearly proved the superiority of the LFSR-based approach over the scan-based architecture. Adopting the novel LFSR architecture resulted in a ~5.6X reduction in toggling activity accompanied by a substantial ~10K pattern reduction and a runtime of nearly ~1.5 hours. Notably, the test power was reduced to 50% showcasing superior efficiency. This approach emerges as the ideal solution for industrial designs providing the best QoR for power, performance, and area. This innovative methodology marks a significant leap toward an energy-efficient and cost-effective VLSI circuit especially for stacked 2.5-3D ICs and chiplets poised to revolutionize chip manufacturing.

Keywords-low-power; chip; LFSR; DFT; test power; 3D; IC

I. INTRODUCTION

Semiconductor scaling has led to the integration of billions of transistors on a single chip to enhance the Integrated Circuit (IC) functionality, as shown in Figure 1. However, this advancement has resulted in a notable increase in test power which is a critical concern in contemporary Ultra Large Scale Integrated Circuit (ULSI) [1]. Larger feature sizes have a substantial impact on testing as circuit complexity grows [2]. To address this challenge, Intel has introduced the FinFET Technology on 2.5D-3D IC [3]. These chipsets provided an alternative to traditional transistor scaling supporting Moore's

law by integrating billions of transistors on a single substrate [4]. Figure 2 illustrates the structure of 2.5D-3D stacking to benefit from routing congestion, and wire delays enabling systems with LP [5]. The features offered by these multi-dimensional chips are smaller size, increased functional density, shorter wiring, reduced interconnect delays, LP consumption, and reduced capacitance. 3D allows heterogeneous SoC designs onto different dies. Despite the aforementioned advancements, these highly integrated designs confront challenges linked to testing complexity and power dissipation, particularly due to the consolidation and packing of multiple ICs onto the same substrate. Hence, the implementation of LP designs remains an ongoing challenge for SoC designers. This challenge arises due to the elevated switching activity during test mode, which results in a substantial increase in power dissipation compared to normal mode operation [10].

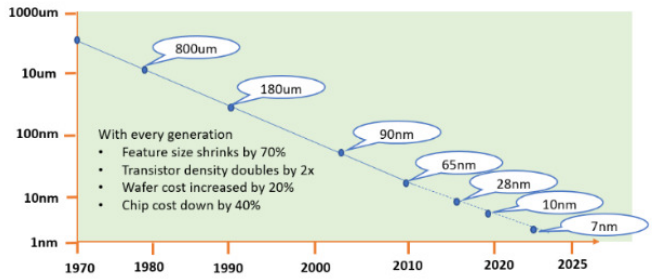

Fig. 1. Technology scaling chart.

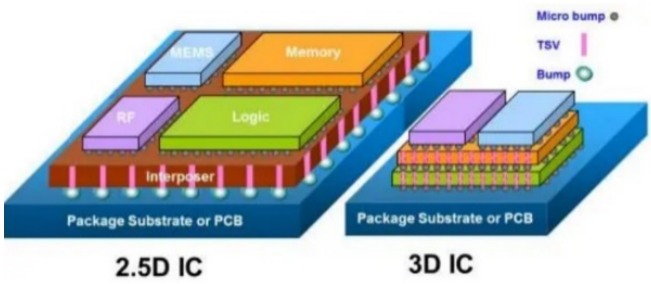

Fig. 2. 2.5D and 3D device structures.

LP testing has become paramount. Chip density with more functionality in the smaller area has led to increased temperature with power density posing risks, such as system failures, diminished performance, potentially permanent damage, jeopardized quality, reliability, yield, and safety, as well as security issues resulting in elevated product costs. Addressing power related concerns emerges as a crucial task for maintaining device performance, longevity, and reliability. Chip testing is a critical endeavor aimed at detecting manufacturing defects and ensuring that chips adhere to the required specifications. This process is trivial for verifying the device's correctness, reliability, and circuit quality at various levels of abstraction typically encompassing circuit, chip, system, and board levels [12]. The 'rule-of-ten' principle underscores the tenfold increase in testing costs advancing to higher manufacturing phase levels [2]. DFT techniques are employed from the circuit level to structurally route out and identify the defects. DFT commonly employs scan-based design techniques to test VLSI/ULSI circuits. This involves incorporating additional circuitry, such as Mux, to transform sequential flops into scan flops. The scan Flip-Flop (FF) latches structural data from the previous chain when enabled to high and functional data from combi-logic and when disabled, as depicted in Figure 3. Thus, it plays a crucial part in loading test vectors and capturing output responses during testing. The tests have paramount importance in VLSI design to ensure the circuit functionality according to the intended designer's spec, with minimized Turn-Around-Time (TAT) and test-escapes [6]. Essential factors in the testing process include run time, power, and coverage during the test. Maintaining testability, namely, controllability and observability, of every node in the circuit is vital for accurate fault detection and diagnosis. This, in turn, enhances the chip's overall quality and reliability. Embracing these principles ensures a robust testing methodology and contributes to cost-effectiveness and timely detection of potential issues. However, Scan designs observe high toggling activity while being in test mode because of the length of scan chains and effective test pattern, which cause a high percentage of functional logic to switch. The result is high stress and power dissipation, which may lead to thermal degradation, chip failure, and escapes on the tester with chip hot spots or chip melts.

Toggling or switching activity mainly occurs when patterns shift in and shift out via scan flops during structural testing. Switching is observed to be greater during the scan/shift testing process than the functional mode of operation due to several factors, as listed below:

1. Uncorrelated test vectors.
2. Non-functional states encountered during the testing phase.
3. Testing of multiple cores with high test compaction.

This increased switching activity leads to an increase in current, manifesting greater power dissipation. Its power can be typically assessed in the Average and Peak components of Power, respectively AP and PP/in the Average Power (AP) and Peak Power (PP) components, respectively [7]. AP is calculated as an average ratio of energy consumed to test time, representing power distribution over time. PP is the maximum power at any moment, which can be caused due to supply voltage drops. This leads to additional gate delays and potentially compromises chip functionality. While high power consumption in a single clock cycle might not exceed thermal limits, prolonged high power can damage the chip. Shift power is the power consumed during scan tests. The power depends on the scan length present in the chain. Capture or functional power refers to the energy used while capturing data. This is performed in one or two cycles based on the static or transition type required according to the test. So, the power observed is always less compared to the scan test. Elevated power during scan operation can cause chips to fail, IR drop, and hot spots in certain regions [7].

LFSRs constitute an alternative that emerges as a versatile digital circuit in the DFT domain for mitigating switching

activity. It has broad applications spanning cryptography, error correction, and pattern generation. Their efficiency is derived from their minimized reliance on combinational logic and their capability to operate at higher frequencies [11]. This configuration empowers LFSRs to generate a pseudo-random sequence of values, rendering them a valuable tool in various domains, particularly in optimizing test patterns and curtailing power consumption during testing processes. Numerous diverse strategies aimed at optimizing power consumption during testing are found in the literature, such as stepped-segment-LFSR [7], single-output-LP-LFSR [8], and multi-output-LP-LFSR techniques for BIST [9]. LFSR re-seeding [10], Gate-Diffusion Input (GDI) [11], Bipolar-Dual reseeding LFSR [12], Dual-Threshold-Bit-Swapping (BS-LFSR) [13], modified LFSR-clock scheme [14], Bit-Swapping-Modified-Clock Scheme (BS-MCS) [15], LP GLFSR [16], and MSS LFSR [17]. However, these structures were not replaced with scan-based designs to power components and DFT behavior completely. This paper proposes a controlled LFSR architecture, focusing on reducing the toggling activity by working on the transitions generated in the design and taking advantage of LFSR superiority over conventional scan structures.

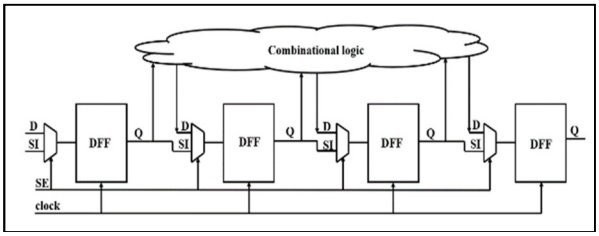

Fig. 3. Scan architecture.

II. STATE-OF-ART TECHNOLOGY

LFSR is depicted in Figure 4 as a shift register housing binary FF with values of 0 or 1. It strategically incorporates XOR gates with a feedback path.

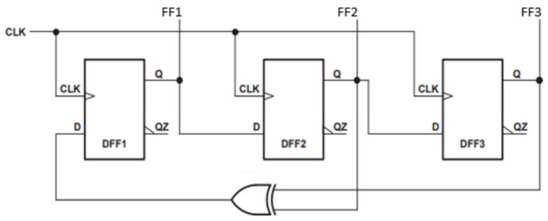

Fig. 4. Linear feedback shift register.

A meticulously designed LFSR possesses the ability to cycle through nearly all possible patterns by navigating distinct 2n-1 states, excluding the all-zero configuration in FF. This class of LFSR, adept at achieving this exhaustive state cycle, is commonly termed as Maximal-Length-LFSR. In matrix terms, the LFSR can be succinctly shown as x_0 (t+1):

$$\begin{bmatrix} x_0\,(t+1) \\ x_1\,(t+1) \\ . \\ . \\ x_{n-1}\,(t+1) \end{bmatrix} = \begin{bmatrix} 0 & 1 & \ldots\ldots & 0 \\ 0 & 0 & \ldots\ldots & 0 \\ . & . & \ldots\ldots & . \\ . & . & \ldots\ldots & . \\ 1 & c_1 & \ldots\ldots & c_n\text{-}1 \end{bmatrix} \begin{bmatrix} x_0(t) \\ x_1(t) \\ . \\ . \\ x_{n-1}(t) \end{bmatrix} \quad (1)$$

The equation in matrix form (1) can be equivalently expressed as:

$$X\,(t+1) = T_s x(t) \quad (2)$$

Expressed as in (2), the relationship X (t+1) is defined, where X (t+1) denotes the current FF output, and x(t) represents the preceding FF output. Examining the provided matrix, Ts takes on the form of a matrix when excluding the initial column and final row. This matrix arrangement vividly illustrates the sequential flow of inputs within the LFSR: x_0 receives input from x_1, then from x_2, and so forth. Notably, the first element in the last row establishes the consistent input received by x_{n-1} from x_0.

$$x_n(t+1) =$$

$$x_0(t) + c_1x_1(t) + c_2x_2(t) + .. + c_{n-1}x_{n-1} \quad (3)$$

$$f(x) =$$

$$1 + c_1x_1(t) + c_2x_2 + c_3x_3 + \cdots + c_{n-1}x_{n-1} + x_n \quad (4)$$

In (3) and (4), the variable c_i denotes the feedback coefficient and x_i are variables. The LFSR can be succinctly articulated through its characteristic polynomial. Notably, the adoption of m-GDI LFSR designs proves effective for LP testing, yielding 30% power reduction [18], a 39% decrease in delay, and a 49% reduction in area [19]. Another approach, proposed in [20], achieves a substantial 65% reduction in test power. Additionally, a gated clock technique, detailed in [21], demonstrates a 10% power reduction, with its efficacy being contingent on the technological parameters of the employed gates. Furthermore, a comparative analysis of the aforementioned techniques was analyzed on the Circuit Under Test (CUT). Among these methods, the Modified Clock Scheme stands out for its effectiveness in minimizing power dissipation [12]. Another innovative technique, introduced in [6], involves Clock Gating (CG) cells, which reduce shift power by gating the clock operation. Furthermore, a comparative study in [10] explores different LFSR types, namely Fibonacci, Galois, and many more LFSR structures. The experimental results unequivocally indicate the superiority of the complete LFSR in achieving optimal power reduction.

III. STRUCTURAL TESTING CONTROLLED BY LFSR

This paper introduces a groundbreaking LFSR-controlled logic architecture engineered to minimize test power by eliminating superfluous toggling/transitions during scan shifting. This approach detailed in this section focuses on achieving noteworthy reductions in power consumption, area, and overall test power through the implementation of the following key methods:

1. Replacement of Scan Flops (SDFF) with LFSR Scan Flops (LFSR-SDFF): During the stitching phase, conventional SDFFs are substituted with LFSR-based

flops, as illustrated in Figure 5. This strategic shift enhances the effectiveness of vector set generation. Each flop within the architecture encompasses inputs, such as SI - Scan-Input, SE – Scan-Enable, D - Data-Input, and Clock, and outputs such as, Q – Scan-Output. Combinational logic is strategically placed between two FF, with Q being placed at the FF output. Integrating LFSRs into the scan chain optimizes the application of test vectors to the circuit, facilitating a more efficient capture and observation of the internal states for fault debugging. This streamlined approach significantly reduces the time required for test pattern generation.

2. Reseeding Techniques Implementation: The incorporation of reseeding techniques further amplifies the effectiveness of the LFSR-driven architecture, ensuring optimal resource utilization and enhancing overall test pattern generation efficiency. Every design has its taps stream-lined based on the scan length.

3. Adoption of Power Gating Techniques for novelty: To address concerns related to higher power consumption in 2.5D/3D ICs, power gating techniques are adopted. By efficiently managing power consumption, these techniques contribute to the architecture's enhanced performance and effectiveness across various IC configurations. By integrating these innovative strategies, the proposed architecture not only streamlines the testing process, but also significantly reduces both the test power and area overhead associated with traditional scan chains. This approach marks a notable advancement in optimizing test pattern generation, ensuring a more efficient application of test vectors and improving the overall effectiveness of fault detection and debugging processes. After the substitution of scan flops with LFSR, the integration of power gates plays a pivotal role in an additional reduction of power consumption. Strategically positioned at the output of each flop, these power gates prove instrumental in regulating switching activity. The shifting process tends to induce a noticeable surge in undesired switching events within the combinational logic, resulting in elevated power consumption. To address this concern, the deployment of power gates is meticulously designed to obstruct the output toggling activity of each scan flop. This proactive measure successfully mitigates excessive switching activity, thereby markedly lowering the overall power consumption.

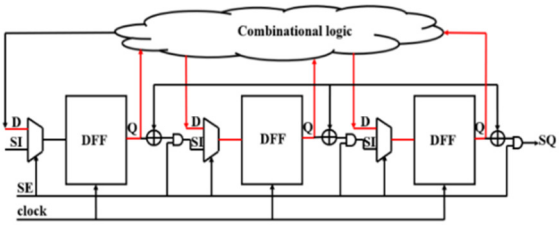

Fig. 5. Example of LP LFSR controlled architecture in functional mode.

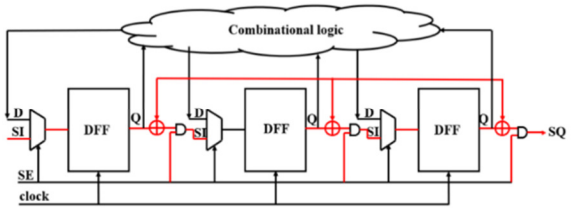

Fig. 6. Example of LP LFSR controlled architecture in test mode.

In the standard operational mode, as depicted in Figure 5, the SE signal is maintained low (SE=0). Data undergo shifting into the FF through the D, with the output being captured via Q. These outputs traverse the combinational logic, feeding the SI of the succeeding SFF. Conversely, SE goes high in test mode, as showcased in Figure 6. Patterns are sampled into the SFF through the SI, and the response is captured through Q. A strategic element named "blockage" is strategically placed at the beginning of the SFF. The former plays a crucial role in minimizing transitions between the test vectors, effectively preventing unnecessary bits from shifting. By doing so, it significantly diminishes the transition activity induced by patterns, ultimately reducing shift power. Moreover, the architecture intelligently bypasses specific combinational logic, thereby eliminating switching activity within the entire combinational circuit and yielding additional savings in shift power. To gauge the effectiveness of this innovative architecture, the ISCAS89 benchmarking circuits, widely acknowledged circuits in the VLSI domain, were employed for validation. Further insights into the efficiency and validation results are provided in Section IV.

TABLE I. TOGGLING ACTIVITY OF DIFFERENT DESIGNS

Design	Test Cov.	Avg. shift WSA %		
		Scan Arc.	LFSR Arc.	Factor
s298	100	38.73	31.50	7.25
s344	100	47.98	45.06	2.93
s526a	99.79	40.51	34.59	5.92
s953	100	38.89	34.79	4.1
S1196	99.97	29.63	27.97	1.66
s1423	99.87	39.95	36.99	2.96
s5378	99.95	51.67	48.81	2.86
s9234	88.91	49.91	44.96	4.95
s13207	99.14	51.48	46.91	4.57
s15850	94.06	56.65	51.07	5.58
s35932	94.18	51.97	47.94	4.03
s38417	99.47	57.19	42.07	15.12
s38584	97.38	50.91	40.36	10.55

IV. EXPERIMENTAL RESULTS

In this section, a novel LFSR architecture is executed and scrutinized utilizing ISCAS'89 benchmark circuits tobe gauged its efficacy. Employing Cadence tools, coverage and test power are meticulously optimized with a minimal pattern set. The scan insertion process was conducted using the Genus tool, while ATPG pattern generation leveraged the Modus tool. The outcomes, as outlined in Table I, elucidate the Weighted Switching Activity (WSA) of diverse designs following the transition from scan to the LFSR-driven architecture. Notably, the switching activity registered a substantial reduction,

averaging a factor of 1.34x. This outcome underscores the superior performance of the proposed approach when compared to the traditional structural-based architecture. Remarkably, the observations made illustrate a consistent reduction in the toggling pattern and create more transitions. This linear behavior holds particular significance in industrial designs, ensuring optimal LP utilization.

Table II shows the substantial runtime reduction of nearly one hour observed in LFSR-driven designs in comparison to their scan-based counterparts. Concurrently, a noteworthy amount of ~4.2K patterns were reduced accentuating the efficiency and practicality inherent in this study's innovative approach. Figure 7 visually depicts the discernible decrease in the switching activity observed across specific benchmarking circuits. The graph serves as a clear representation of the reduction in switching/toggling activity accomplished by the proposed LFSR architecture, highlighting its efficacy in comparison to the conventional scan-based approach. It is also articulated from Table II that the factor ranges from 2.42x folds for smaller node designs to 9.55 for convoluted designs, which hold higher nodes in the design. With the increase in design nodes, the complexity of the design is also elevated, and the novelty exhibits an elevated reduction in the switching power by the factor of X folds. This behavior is ideal for the adaptation of multi-dimensional ICs, like 2.5D and 3D ICs.

TABLE II. SHOWS QOR METRICS OF DESIGNS

ISCAS	Design	Coverage (%)		# of Patterns	Run time (h: min)	Power (in MW)
s13207	Existing Scan Arc	Logic	97.56	5117	1:59	1612.07
		Delay	79.65	4345	1:42	
	BS-LFSR	Logic	97.41	4923	2:09	1810.45
		Delay	75.23	5234	1:57	
	Novel LFSR Arc	Logic	99.10	3289	1:02	1123.01
		Delay	85.09	4091	1:19	
s38417	Existing Scan Arc	Logic	89.03	4983	1:29	1456.15
		Delay	65.70	7664	2:09	
	BS-LFSR	Logic	87.76	5012	1:43	1753.02
		Delay	61.41	8124	2:31	
	Novel LFSR Arc	Logic	94.24	3632	0:59	1243.54
		delay	71.08	6454	1:57	
s38584	Existing Scan Arc	Logic	90.23	2012	0:35	958.45
		Delay	79.59	1873	0:40	
	BS-LFSR	Logic	89.14	2307	0:50	1034.87
		Delay	75.25	2003	0:59	
	Novel LFSR Arc	Logic	94.45	1086	0:27	595.34
		Delay	86.71	1697	0:52	

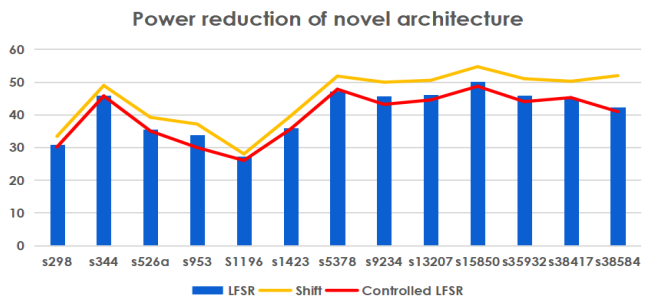

Fig. 7. Effective reduction in transitions shown across LFSR, shift, and controlled LFSR designs.

The QoR, such as runtime, test coverage, pattern count, and power, are some of the dominant parameters performing well in LFSR when compared to scan-based testing. LFSR ensures the protection of the data from vulnerable activities and data breaches. The scan-based testing does not certify that data are protected and is more susceptible to data breaches. This LFSR-based novelty proved to be more volatile in terms of exhibiting better QoR and scan protection. In Table II, the results of the novel LFSR architecture are incorporated on real-based SoC designs of ISCAS'89 benchmarking circuits and they are compared with the existing scan-based architecture and BS-LFSR architecture presented in [27]. From the populated table, it is obvious that the QoR metrics, i.e., power, runtime, pattern count, and test coverage, were all found to be reduced compared to the existing architectures. Figure 8 shows the major power reduction of the LFSR-based architecture over the traditional scan-based architecture.

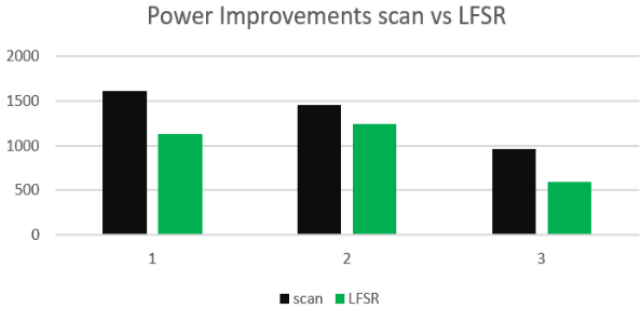

Fig. 8. Power reduction of Scan Vs LFSR controlled architecture.

TABLE III. SUMMARY OF RESULTS

Parameter	Factor
Toggling activity	Reduced by 5.6X
Toggling activity variation	2.42X to 9.55X and dependent on the number of nodes in the design
Pattern reduction	~ 10k
Coverage	Increased by an average of 3.76% for static test 7.51% for delay test 0.59% for scan test
TAT	~1.5 hours to a few minutes
Power reduction	50%

Table III presents the summarized results, where the LFSR-driven approach exhibited a substantial 1.34X reduction in toggling activity, which is accompanied by a remarkable 4K pattern reduction and a runtime acceleration of nearly 1 hour compared to traditional scan-based designs. The test power witnessed a reduction of approximately 45%, showcasing superior outcomes in power efficiency, runtime, coverage, and pattern count.

V. CONCLUSIONS AND FUTURE SCOPE

The focus of the current paper is oriented toward the testing of various benchmarking designs to showcase and evaluate the performance of the scan Vs novel architecture. In this study, a groundbreaking Linear Feedback Shift Register (LFSR)-driven architecture is introduced. Displaces scan Flip-Flops (FF) at the 45 nm technology level using Cadence Design For Test (DFT)

solution, namely Genus-Modus, on benchmarked ISCAS'89 circuits. The experimental results are located between the novelty of the proposed LFSR-driven architecture and conventional scan-based designs as well as existing BS-LFSR techniques. Importantly, the study unveiled a linear relationship between design complexity and the efficacy of the proposed innovation, signaling its practical suitability given industrial applications, like 2.5D and 3D ICs. This work is further extended to hyper convoluted industrial Silicon-on-Chip (SoC) designs scaled down to 10 nm - 7 nm SoC designs. Scan structures encompassing scan chains present security challenges that may result in potential confidential data leaks and unauthorized access through standard test interfaces, such as IEEE 1500 and IEEE 1149X. Safeguarding sensitive information, ensuring authorized data integrity, and preventing unauthorized module operation are of utmost importance [10]. To address these concerns and bolster scan security, LFSR is an ideal strategy which readers can further orient on.

REFERENCES

[1] K. B. Reddy, A. S. Priya, E. L. Prasad, and S. Kamatchi, "Reduction of Toggling Activity Using Novel LFSR Driven Logic for ULSI Circuits," in *2023 International Conference on Next Generation Electronics (NEleX)*, Sep. 2023, pp. 1–5, https://doi.org/10.1109/NEleX59773.2023.10421291.

[2] A. S. Priya, K. S, and E. L. Prasad, "Early Register Transfer Level (RTL) power estimation in real-time System-on-Chips (SoCs)," *Journal of Integrated Science and Technology*, vol. 11, no. 1, pp. 454–454, 2023.

[3] A. Swetha Priya, S. Kamatchi, and E. Lakshmi Prasad, "Estimation of SoC Testability at Early RTL Stage," in *Intelligent Manufacturing and Energy Sustainability*, Singapore, 2023, pp. 339–367, https://doi.org/10.1007/978-981-19-8497-6_33.

[4] A. S. Priya and K. S, "Power Optimization of VLSI Scan under Test using X-Filling Technique," in *2021 Emerging Trends in Industry 4.0 (ETI 4.0)*, Feb. 2021, pp. 1–9, https://doi.org/10.1109/ETI4.051663.2021.9619269.

[5] A. S. Priya, "Defect-aware methodology for low-power scan-based VLSI testing," *2015 Conference on Power, Control, Communication and Computational Technologies for Sustainable Growth (PCCCTSG)*, pp. 234–238, Dec. 2015, https://doi.org/10.1109/PCCCTSG.2015.7503931.

[6] S. V, S. Raghav, and A. J. P, "Efficient don't-care filling method to achieve a reduction in test power," in *2015 International Conference on Advances in Computing, Communications, and Informatics (ICACCI)*, Dec. 2015, pp. 478–482, https://doi.org/10.1109/ICACCI.2015.7275654.

[7] B. L. Dokic, "A Review on Energy Efficient CMOS Digital Logic," *Engineering, Technology & Applied Science Research*, vol. 3, no. 6, pp. 552–561, Dec. 2013, https://doi.org/10.48084/etasr.389.

[8] M. D. Savio. M *et al.*, "VLSI Architectures for Security Analysis with Dual-Key LFSR Using Barrel Shifter and S-Box," in *2023 International Conference on Recent Advances in Electrical, Electronics, Ubiquitous Communication, and Computational Intelligence (RAEEUCCI)*, Apr. 2023, pp. 1–5, https://doi.org/10.1109/RAEEUCCI57140.2023.10134034.

[9] N. Mathan, L. Magthelin, M. Malathi, G. I. Shamini, M. A. Muthiah, and T. Ravi, "Analysis of an Efficient Fault Tolerant Linear Feedback Shift Register for Low Power Applications," in *2024 10th International Conference on Communication and Signal Processing (ICCSP)*, Apr. 2024, pp. 937–942, https://doi.org/10.1109/ICCSP60870.2024.10543614.

[10] S. Ahmadunnisa and S. E. Mathe, "Multi-LFSR Architectures for BRLWE-Based Post Quantum Cryptography," *IEEE Access*, vol. 12, pp. 96258–96272, 2024, https://doi.org/10.1109/ACCESS.2024.3426990.

[11] S. Hussain, A. K. Chaudhary, and S. Verma, "Design of Secured Lightweight PRNG Circuit using LFSR for Portable IoT Devices," in *2022 Third International Conference on Intelligent Computing Instrumentation and Control Technologies (ICICICT)*, Dec. 2022, pp. 1588–1592, https://doi.org/10.1109/ICICICT54557.2022.9917644.

[12] I. Pomeranz, "Positive and Negative Extra Clocking of LFSR Seeds for Reduced Numbers of Stored Tests," in *2021 IEEE 30th Asian Test Symposium (ATS)*, Aug. 2021, pp. 109–114, https://doi.org/10.1109/ATS52891.2021.00031.

[13] M. Saikia and B. P. Shrivastava, "Adaptive Reconfigurable LFSR: Dynamic Tapping and Reseeding for Enhanced Pseudo Random Number Generation," in *2024 IEEE International Students' Conference on Electrical, Electronics and Computer Science (SCEECS)*, Oct. 2024, pp. 1–6, https://doi.org/10.1109/SCEECS61402.2024.10482241.

[14] J.-C. Ying, W.-D. Tseng, and W.-J. Tsai, "Bipolar Dual-LFSR Reseeding for Low-Power Testing," in *2018 IEEE Conference on Dependable and Secure Computing (DSC)*, Sep. 2018, pp. 1–7, https://doi.org/10.1109/DESEC.2018.8625105.

[15] R. Trivedi, S. Dhariwal, and A. Kumar, "Comparison of various ATPG Techniques to Determine Optimal BIST," in *2018 International Conference on Intelligent Circuits and Systems (ICICS)*, Apr. 2018, pp. 93–98, https://doi.org/10.1109/ICICS.2018.00031.

[16] S. B. Jambagi and S. S. Yellampalli, "Exploration of Various Test Pattern Generators for Power Reduction in LBIST," in *2017 International Conference on Current Trends in Computer, Electrical, Electronics, and Communication (CTCEEC)*, Sep. 2017, pp. 710–713, https://doi.org/10.1109/CTCEEC.2017.8455062.

[17] M. Mosalgi and G. Hegde, "Power Optimized TPG for BIST Architecture," in *2017 IEEE International Conference on Computational Intelligence and Computing Research (ICCIC)*, Sep. 2017, pp. 1–4, https://doi.org/10.1109/ICCIC.2017.8524577.

[18] V. Thirunavukkarasu, R. Saravanan, and V. Saminadan, "Performance of low power BIST architecture for UART," in *2016 International Conference on Communication and Signal Processing (ICCSP)*, Apr. 2016, pp. 2290–2293, https://doi.org/10.1109/ICCSP.2016.7754103.

[19] L. Shaer, T. Sakakini, R. Kanj, A. Chehab, and A. Kayssi, "A low power reconfigurable LFSR," *2016 18th Mediterranean Electrotechnical Conference (MELECON)*, pp. 1–4, Apr. 2016, https://doi.org/10.1109/MELCON.2016.7495422.

[20] R. Sharma and B. Singh, "Design and analysis of linear feedback shift register(LFSR) using gate diffusion input(GDI) technique," *2016 5th International Conference on Wireless Networks and Embedded Systems (WECON)*, pp. 1–5, Oct. 2016, https://doi.org/10.1109/WECON.2016.7993424.

[21] T. Patil and A. Dhankar, "A review on power optimized TPG using LP-LFSR for low power BIST," in *2016 World Conference on Futuristic Trends in Research and Innovation for Social Welfare (Startup Conclave)*, Oct. 2016, pp. 1–4, https://doi.org/10.1109/STARTUP.2016.7583923.